Co-evolutionary Approach to Reduce Soft Error Rate of Implemented Circuits on SRAM-based FPGA

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Abstract

Soft errors such as Single Event Upset (SEU) have great effect on performance degradation of circuits implemented on SRAM-based FPGA. The soft error in configuration bits which control the logic and routing parts of the circuit, leads to permanent faults. In this paper, we have developed a co-evolutionary method to reduce the effect of soft error on the implemented circuit on FPGA. This method is based on cooperation of genetic algorithm and ant colony optimization. The efficiency of co-evolutionary method has been proved by comparison of its results with the proposed genetic algorithm and ant colony optimization. The experimental results for some MCNC benchmark circuits show up to 34% improvement compare to genetic algorithm and up to 60% improvement against ant colony optimization.

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Index Terms

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Keywords

Soft error rate, SRAM_based FPGA, Place and route, GA, ACO