Abstract

This paper is concerned about microprocessor compatible PWM generator architecture by using
Field Programmable Gate Array (FPGA). In PWM the variation of duty cycle change the width of
the pulse. The PWM generator (PWMG) is interfaced to the bus of a microprocessor. The
microprocessor initiates PWMG to specify duty cycle. The duty cycle remain unchanged until
new data available to the PWMG from microprocessor unit. The output signal of PWMG is logic
“1” and logic “0” for a specific time period. The architecture has been designed with VHDL code
and verified using Xilinx ISE Design Suite 14.7. The design is successfully implemented on
SPRATAN-6 FPGA board. The operating frequency of this proposed architecture is of
292.650MHz.

References


Index Terms

Computer Science
Circuits and Systems

Keywords

Duty cycle, Microprocessor, PWM, VHDL, FPGA