Abstract

New methodologies for efficiently describing and implementing digital systems are investigated as the complexity of binary digital hardware system is relentlessly expanding. From the recent study, it is shown that multi valued logic approach is more advantageous over existing binary digital system. Ternary means a multilevel switching component, which switches between 3 levels. Recent study on ternary number system (TNS), has shown numerous advantages over binary. In recent times, Double Base Number Systems (DBNS) are considered as alternatives to binary number system because of their capabilities of performing partial product free multiplications. On the other hand, Double Base Ternary Number System (DBTNS) multipliers are efficient compared to conventional TNS multiplier. High performance digital signal processing systems which can able to handle all Digital Signal Processing (DSP) algorithms, broadly utilize Multiply-Accumulate (MAC) operation. So, TNS Adder and DBTNS Multipliers can be used to implement fast MAC units. Keeping this in view, a new approach of designing efficient MAC unit using DBTNS multiplier is proposed in this work. The performance of proposed MAC unit is compared with conventional ternary multiplier-based MAC unit and they
are mapped on a FPGA chip. Performance analysis clearly indicates that the supremacy of the proposed architecture over conventional ternary multiplier-based MAC unit.

References


Index Terms

Computer Science Wireless

Keywords

Ternary Number System (TNS); Trit; Ternary Gates; Ternary Arithmetic; Double Base Ternary Number Systems (DBTNS); DBTNS Multiplier; Multiply and Accumulate Unit (MAC); FPGA; DSP Algorithms.