Effective Techniques for Performance Enhancement on Embedded Multi-Processor Architectures

International Journal of Computer Applications
Foundation of Computer Science (FCS), NY, USA

Volume 181
Number 17

Year of Publication: 2018

Authors:
Hassan Salamy

10.5120/ijca2018917834
{bibtex}2018917834.bib{/bibtex}

Abstract

As the complexity of embedded applications is ever increasing, the trend in embedded architecture is to utilize a multi-processor system on a chip (MPSoC). MPSoCs provide the compute power and flexibility to effectively execute complex embedded systems. An embedded system often execute multiple complex embedded applications simultaneously. In this article, we tackle two main problems to further enhance the effective utilization of the embedded MPSoC architecture to reduce the execution time of the applications, namely, resource allocation and scheduling. We first present an effective resource allocator that examines the nature of the applications in the system to fairly allocate the fast on-chip scratchpad memory budget and the processing elements. Then this article presents an effective task scheduler that integrates scheduling and on-chip scratchpad memory partitioning for the maximum optimization of the system. Results on multiple real and synthetic benchmarks showed the effectiveness of our techniques.

References


**Index Terms**

Computer Science  
Embedded Systems

**Keywords**

MPSoC, scratchpad, task scheduling, resource allocation.