Abstract

More than 50% of random logic power in an SOC chip is typically consumed by Flip Flop. This is because of redundant transition of internal nodes, when the input and output appear to be in the same state. Different low power techniques have been proposed, but all of these designs use more transistors. Leading to an increase in size, which is too costly since flip flops typically account for 50% of random logic area. In this paper we design D flip-flop using 2x1 multiplexer which has reduced transistor count compared to other low power designs of D flip-flops. The focus is to design high speed, low power consumption, positive edge triggered conventional D flip-flop which can be used for registers in multipliers. In this paper the D flip-flop is modified in such a way that it controls the overall capacitances during the operation and will optimize the total capacitance that results in the decrease of the Average Power dissipation. The flip-flop is realized using only 8 transistors. The circuit is characterized by using cadence tools in 0.18 µm technology.

References
Design and Implementation of Conventional D Flip-Flop for Registers

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Index Terms

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Keywords

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