Design and Implementation of Conventional D Flip-Flop for Registers

A. Lakshmi
Department of ECE
KMIT
Hyderabad, India

P. Chandrasekhar Reddy, PhD
Department of ECE
JNTUH
Hyderabad, India

ABSTRACT
More than 50% of random logic power in an SOC chip is typically consumed by Flip Flop. This is because of redundant transition of internal nodes, when the input and output appear to be in the same state. Different low power techniques have been proposed, but all of these designs use more transistors. Leading to an increase in size, which is too costly since flip flops typically account for 50% of random logic area. In this paper we design D flip-flop using 2x1 multiplexer which has reduced transistor count compared to other low power designs of D flip-flops**.** The focus is to design high speed, low power consumption, positive edge triggered conventional D flip-flop which can be used for registers in multipliers. In this paper the D flip-flop is modified in such a way that it controls the overall capacitances during the operation and will optimize the total capacitance that results in the decrease of the Average Power dissipation. The flip-flop is realized using only 8 transistors. The circuit is characterized by using cadence tools in 0.18 µm technology.

Keywords
D flip-flop, registers Cadence Tool, CMOS circuit, 2x1 Multiplexer

1. INTRODUCTION
Billions of transistors can be integrated with the new development of CMOS technology, allowing the design on a single chip. The increasing complexity and high performance requirements of mobile devices have the power consumption problem in all abstraction levels. The main power consumption consists of dynamic and static power. Dynamic power is the most dominant power dissipation in CMOS VLSI circuits [1- 4].It is caused by the switching activities of the circuits. The dynamic power dissipation is due to the charging and discharging of the node capacitances is given by:

$$C_n = 0.5 C V_{dd}^2 \quad E\,sw \quad f_{clk} \qquad (1)$$

Where C is the physical capacitance of the circuit, V_{dd} is the supply voltage, E(sw) (referred as the switching activity) is the average number of transitions in the circuit per $1/f_{clk}$ time, and f_{clk} is the clock frequency. Power consumption is reduced by any one of the factor. The voltage scaling is the effective way for reducing power consumption .Multi supply voltage technique is upcoming technique to reduce the dynamic

Power without degrading the other performance [5].In order to interface different voltage levels in multi voltage technique; the additional circuit like level shifter is required. Transistor sizing is much significant method for the modifying the of circuit performance to avoid the area constraint. The proper sizing of transistor is required for fair evaluation of the power consumption [6-7]. The intention of the optimization is to reduce the power-delay product or the energy utilization. The power and delay depends on the transistor sizes which are proportional of R^n ($w \in R^n$) as is the transistor count. In this paper new D flip-flop with transistor sizing is used to reduce the power in the circuit level optimization.

The prevailing design philosophy requires that activities taking place in various portions of a circuit be synchronized with respect to a global signal. This global signal is usually called the clock. Chief among these synchronizing elements are latches and flip-flops, which remember the previous input until new data is applied and the clock is asserted. Although latches and flip-flops owe their existence and popularity to synchronous design, the first latches and flip-flops were asynchronous and used separate signals to set and reset the data [1].

The difference between latches and flip-flops is the position of the clock at which the input is transmitted to the output. Latches are level sensitive or pulse triggered, that is to say they require that the clock be at the proper logic level before the input is transferred to the output. Flip-flops on the other hand are edge triggered. They require a positive or negative transition of the clock to latch the input. A positive edge-triggered flip-flop latches the input on the low to high going edge of the clock, while a negative edge triggered flip-flop perform its latching on the negative going edge of the clock.

Designing large asynchronous circuits and ensuring their functionality over all process corners is no mean feat. To ensure robust design, it is best to synchronize all activities with respect to a single global clock. Because the output of the circuits must be sampled and stored at each clock edge to provide a stable set of inputs to subsequent circuits, the role of latches and flip-flops grew in importance. This shift led to the design of the clocked SR latch shown in figure 1.

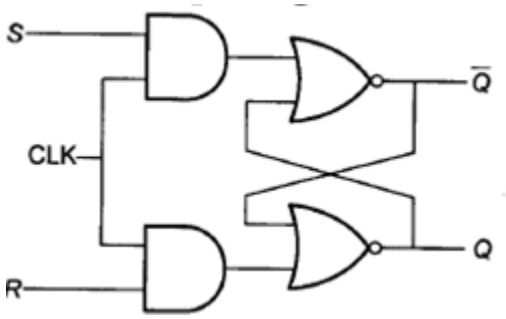


Fig.1: Clocked S-R Flip-Flop

Because latches and flip-flops in synchronous circuits were used mainly as delay elements to buffer input, the word latch and flip-flop become synonymous with the D- latch and flip-flop

Flips-flops and latches are some of the most frequently used elements in digital VLSI systems. In synchronous systems, flip-flops are the starting and ending points of signal delay paths, which decide the maximum speed of the systems. Since, they are clocked at the system operating frequency; flip flops consume a large amount of power [7]. About 30%-70% of the total power in the system is dissipated due to clocking network, and the flip-flops [3].

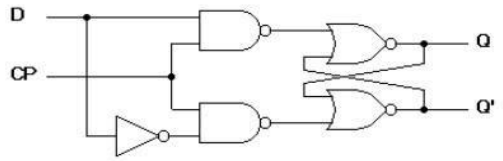
Flip-flops and latches are indispensable components of every sequential system. A large portion of the clock power is used to drive these sequential elements. Reducing the clock power dissipation of flip-flops and latches is thus a prime concern for the total chip power reduction.

2. TRANSISTOR SIZING

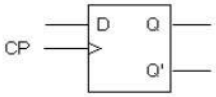
Different techniques are applied for power optimization in CMOS VLSI circuits. Transistor sizing is very important for the determination of circuit performance [5-6].As a result for providing reasonable evaluation, an optimal size of transistor is necessary. The aim of the optimization is to minimize the power-delay product or the energy consumption of the circuit. The polynomial method is utilized [6] for transistor sizing. The heuristic algorithm is applied [7] for sizing the width of NAND, MUX and INV Gates. The power and delay depend on the transistor sizes which are relative of *Rn* ($w \in Rn$)as is the transistor count. In fact, the transistor sizing algorithm tries to optimize a goal in *n* +1 dimension space. That is, n dimensions are related by *K s i* ' and then +1th is the goal which is optimized [6-7].The load capacitance of the circuit can be reduced by optimizing the transistor size. In general, increasing the transistor sizes results in a large discharging current and simultaneously increases the parasitic capacitance. On the other hand, reducing the transistor sizes will result in declining input capacitance that may be the load capacitance for other gates and lowering the speed of the circuit. Thus, the purpose of transistor sizing is to obtain the minimum power dissipation under certain performance requirements. This technique is implemented in the D flip-flops and registers are implemented using various D flip-flops.

3. D FLIP-FLOP

Flip-flops appear in various configurations, such as J-K flip-flops, D-flip-flops and T-flip-flops, where the D-flip flop is most commonly used. A conventional single edge triggered (SET) flip flop typically latches data either on the rising edge or falling edge of the clock cycle. The d-flip flop is called as data flip flop or delay flip flop. A flip –flop is an electronic circuit that has 2 stable states 0 and 1.A single flip flop is capable of serving as one bit of memory. The logic diagram of clocked D flip-flop with Nand gates, its graphical symbol and transition table are shown in figure



(a) Logic diagram with NAND gates



(b) Graphical symbol

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

(c) Transition table

Clocked D flip-flop

Fig.2: Clocked D Flip-Flop

4. PROPOSED METHOD

The proposed study is to design, the conventional positive edge triggered D- flip flop in a 0.18 µm CMOS technology. Previous to this, there are few designs but not more suitable for optimization techniques. So we are designing a new Methodology to design D flip flop using 2x1 MUX. By using this technique the required percentage of power consumption is low and also the speed of performing the procedure is high.

The proposed study is to design, the conventional D flip-flop in a 0.18µm CMOS technology.

The various steps involved in the design flow are as follows:

- Creating CMOS schematics using virtuso Schematic composer
- Symbol creation for the schematic using Symbol editor
- Test bench for CMOS schematic simulation using Analog design environment(ADE) with Spectre simulator
- CMOS physical (Layout) design using virtuso layout editor
- DRC check using Diva/Assura Design Rule Checker
- Layout extraction using Diva/Assura circuit Extractor
- Layout Vs Schematic verification
- Composite test bench creation using hierarchy editor
- Post Layout simulation using ADE with Spectre simulator

Technology used is 0.18 µm

- CMOS N well process

- 6 metal layers
- single poly
- NMOS Transistor

  width = 0.6 µm

  length =0.18 µm

  PMOS Transistor

  width=1.2µm

  length=0.18 µm

Design rules for 0.18 µm technology (λ =0.1um)

N-Well	**In term of µm**	**In term of λ**
Min N-well width	1.0µm	10 λ
Min N-well separation	1.0µm	10 λ
Min N-buried enclosure	0.3µm	3 λ
P-Well		
Min P-well width	1.2µm	10 λ
Min P-well separation	1.0µm	10 λ
Min N-buried enclosure	0.3µm	3 λ
Poly		
Min Poly width	0.2µm	2 λ
Min Poly spacing	0.3µm	3 λ
Min Poly ext bey ox	0.4um	4 λ
Min Poly ext bey gate	0.2µm	2 λ
Contact		
Min contact width	0.2µm	2 λ
Min contact spacing	0.2µm	2 λ
Min ox en of contact	0.2µm	2 λ
Metal-1		
Min metal1 width	0.3µm	3 λ
Min metal1 spacing	0.3µm	3 λ
Min metal1 en of contact	0.1µm	1 λ
Via-1		
Min and Max width of via1	0.2µm	2 λ
Min via1 spacing	0.3µm	3 λ
Min metal1 en of via1	0.1µm	1 λ

4.1 Design Implementation

Conventional D flip-flop is designed using cadence virtuso tool. This Proposed schematic is aimed for using in registers in multipliers. The Schematic circuit is shown in the figure 3.The schematic is created using virtuso Schematic composer

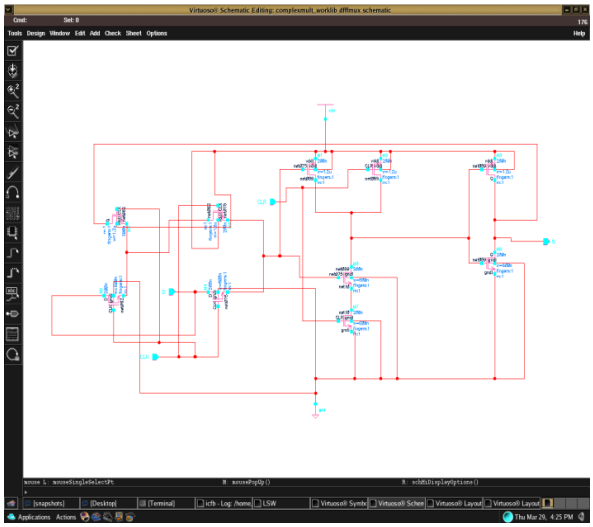


Fig.3: Proposed Conventional D Flip-Flop

Figure 3 shows the schematic of D flip - flop using 5 PMOS and 5 NMOS transistors. The circuit uses 2x1 Mux, two input NAND gate and inverter.2x1 Mux is again designed as shown in the figure 4.Its Schematic is created using virtuso schematic composer.

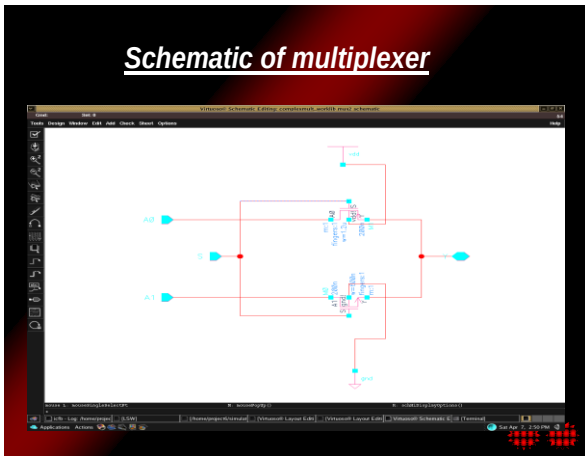


Fig.4: Schematic of 2x1 Multiplexer

The two inputs of the multiplexer are D and previous Q, select signal is raising edge of the clock. Here Multiplexer is designed using only two transistors. One NMOS transistor and one PMOS transistor. For Rising edge of the clock Multiplexer selects D and for falling edge of the clock Multiplexer selects previous Q of the D flip-flop. The Symbol creation for the schematic of figure 4 is done using Symbol editor. The symbol for 2x1 multiplexer is shown in figure 5 .

Two input NAND gate is designed using two NMOS transistor and two PMOS transistors. The inputs of this NAND gate are clear signal and output of Multiplexer. The output of NAND gate is fed to inverter and the output of inverter is Q .Inverter is CMOS Inverter.

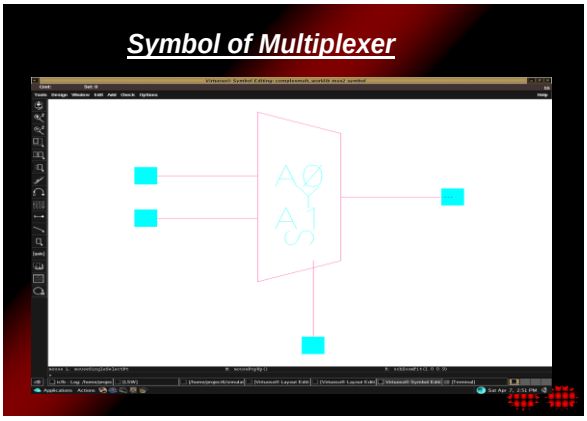


Fig.5: Symbol of 2x1 Multiplexer

The Symbol creation for the schematic of figure 3 is done using Symbol editor. Test bench for CMOS D flip-flop schematic simulation is done using Analog design environment (ADE) with Spectre simulator.

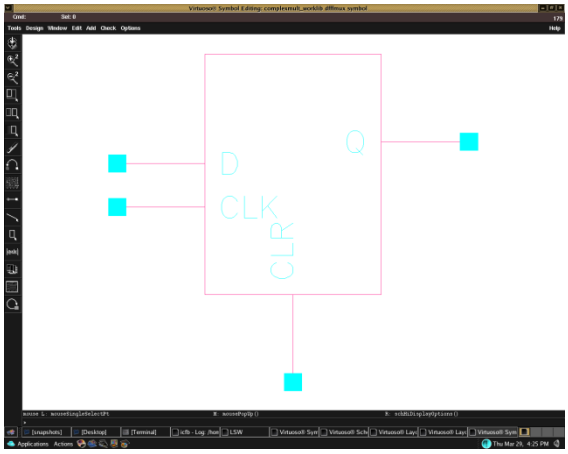


Fig.6: Schematic of Conventional D Flip-Flop

Physical (Layout) design using virtuso layout editor is done for D flip- flop and is shown in the figure 7.Design rules are checked and the layout is extracted, where optimization can be done at this level.Verification is done using LVS. Post Layout simulation is done using ADE with Spectre simulator

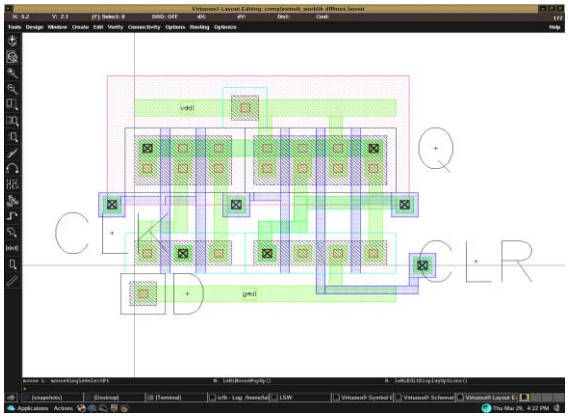


Fig.7: Layout of Proposed Conventional D Flip-Flop

5. RESULTS AND DISCUSSION

In the first phase, Multiplexer is implemented in 0.18 µm submicron technology. Then the width of the transistor is changed to get the optimized power using HSPICE optimizer. The width is varied from 2µm to 100nm for the transistor. Among all Multiplexers it consumes less power and Delay than other multiplexers.

In the second phase, D flip-flop is implemented and its performances are analyzed. The functionality of the circuit is verified in all combinations of input. Figure.8. shows the output waveforms of the D flip-flop.

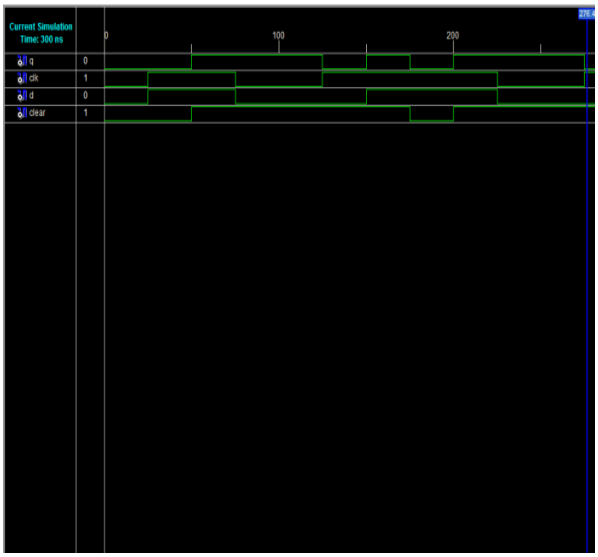


Fig.8: Simulation Results of a conventional D Flip-Flop

6. CONCLUSION

Multiplier is the heart of DSP processor. In this paper D Flip-Flop is designed using Multiplexer, AND and Inverter and is simulated at 0.18 µm technology. It is designed with transistor sizing and their performances are studied at 0.18 µm technology library file. The proposed D flip-flop is used for designing the registers used in multipliers. Then different multipliers can be implemented using this design. Power and delay performance are analyzed and compared with other D Flip Flops .Multiplier using those registers built with proposed D Flip- Flop will have high performance.

7. REFERENCES

[1] Massoud Pedram., 1995 Design Technologies for Low Power VLSI, Encyclopedia of Computer Science and Technology,

[2] Gray Yeap and Gilbert, 1998 Practical Low power Digital VLSI Design, Kluwer Academic Publishers.

[3] Rabaey.J, 2003 Digital Integrated Circuits: A Design Perspective, 2nd edition, Prentice-Hall.

[4] Pedram, . 1996,Power Minimization in IC Design, ACM Transactions on Design Automation of Electronic Systems, Vol 1, No. 1, pp. 3-56

[5] Jui-Ming Chang and Massoud Pedram. 1997,Energy Minimization Using Multiple Supply Voltages", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 5, No. 4, Pp: 436-444,

[6] J. P. Fishburn and A. E. Dunlop, 1985, TILOS: a posynomial programming approach to transistor sizing," in Proceedingsof the International Conference on computer Aided Design(ICCAD '85),

[7] Yu Chien-Cheng "Design of Low-Power Double Edge-Triggered Flip- Flop Circuit" 2007 Second IEEE

Conference on Industrial Electronics and Applications 23-25 May 2007 pp 2054-2057

[8] Nedovic, N. Aleksic, M. Oklobdzija, V.G. " Comparative analysis of double-edge versus single-edge triggered clocked storage elements" Circuits and Systems 2002, ISCAS 2002.,IEEE International Symposium

[9] Vladimir Stojanovic andVojin G.Oklobdzija, Comparative, "Analysis of Master-Slave Latches and Flip-Flops for High–Performance and Low- Power System," IEEE J. Solid-State Circuits, vol.34, pp.536-548, April 1999.

[10] R. Hossain, L. D. Wronski, and A. Albicki, "Low power design using double edge triggered flip-flops," IEEE Trans. on VLSI Systems, vol. 2, no. 2, pp. 261-265, June 1994.

[11] Yiran Li, Tie Sun, Xiaodong Yang, Zhenming Zhou "A Comparative Analysis of Single Edge-Triggered & Dual Edge-Triggered Flip-Flops"

[12] N.H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A System Perspective, 2nd ed. Reading MA: Addison-Wesley, 1993

[13] Gary K.Yeap, Practical Low power Digital VLSI Design, Kluwer Academic Publishers, 1998.

[14] Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design 3RD Edition TATA McGRAW HILL.