Performance Evaluation and Assessment of LDPC Codec over DVB-S2 and WLAN802.11n Applications

Noor S. Enad
Department of Communication Engineering
College of Electronics Engineering
University of Mosul
Mosul, Iraq

Mohammed H. Al-Jammas, PhD
Computer & Information Engineering Dept.
College of Electronics Engineering
Ninevah University
Mosul, Iraq

ABSTRACT
Low-Density Parity-Check (LDPC) codes are higher coding gains, the performance of LDPC code are closed to the Shannon limit, this make the decoding very attractive to many applications in digital communication systems, like DVB-S2 and WLAN802.11n, in this work the performance of LDPC code evaluated in different block lengths, code rates and number of iterations and implemented in MatLab simulation. In this work, a random signal is generated and encoded by multiplying the information by a matrix in the encoder, the resulting codeword modulated using BPSK modulation, codeword transmitted over an AWGN channel. This process implemented over different Eb/N_0 values.

Keywords
LDPC Code, DVB-S2, WLAN802.11n

1. INTRODUCTION
As the signal transfer from the transmitter to the receiver it will suffer from the channel conditions as interference, noise and fading, this causing signal errors which make its recovery at the receiver impossible somewhat. Some techniques developed to help the receiver recover the original signal. There are two types of error correction techniques, ARQ (Automatic Repeat Request) and FEC (Forward Error correction). In ARQ, when the recipient discovers an error in the information received, a re-sending is request. In most circumstances, it is not possible to re-send data, FEC Is the appropriate alternative where redundant bits are added to the data, these redundant bits don't have any new information but used later in detecting and correcting the error according to a certain algorithms at the receiver [1]. The process of adding redundant bits called channel coding. Channel coding is one of DSP techniques used to improve communication performance under inappropriate conditions [2].

2. LOW DENSITY PARITY CHECK (LDPC) CODE
LDPC code one of forward error correction codes invented by Robert Gallager in 1960[1]. Because the hardware implementation complexity at that time it is ignored until it is rediscovered by MacKay and Neal at 1996[3]. It considered capacity-approaching codes. The name low-density come from its parity check matrix in which the number of ones much less than the number of zeroes, also called Gallager codes. It is regard one of block codes type in which the message divided in to blocks everyone has K information bits, which encoded and decoded alone [4]. LDPC code consists of two matrices, generator matrix (G-matrix) at the encoder and parity check matrix (H-matrix) at the decoder. Unlike the other block codes, in LDPC code, H-matrix is generated first and from H-matrix, G-matrix is generated [5]. LDPC code has wide applications as in satellite communication (DVB-S2), storage devises, optical communications, Wi-Fi and mobile WiMax [6] and it's chosen to be the channel coding type for the next generation of mobile system 5G for data transmission channel [7].

2.1 LDPC Code Representation
There are two methods to represent LDPC code, matrix representation and tanner graph [8].

2.1.1 Matrix Representation
LDPC code is defined by its parity check H-matrix. H-matrix has dimensions of $n * m$, where n is the number of rows and m is the number of columns. Number of ones in this matrix must be less than number of zeros so much. If number of ones in rows is W_r and number of ones in columns is W_c, so $w_r \ll n$ and $w_c \ll m$. As shown below.

$$\mathbf{H} = \begin{bmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix}$$

2.1.2 Tanner Graph
Tanner Graph is a graphical way to represent a parity check matrix of LDPC code. This graph can give a full description for LDPC code and help to understand the decoding process. It's called bipartite graph, which means that nodes cannot connect with node have the same type. The rows of H-matrix represent check nodes (c-nodes) and columns represent variable nodes (v-nodes).

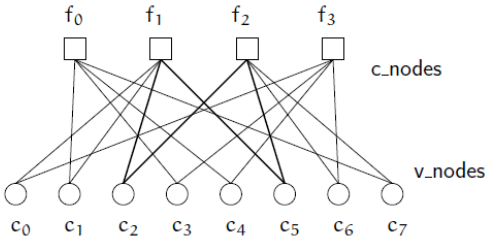

Figure (1): Tanner Graph.

C-nodes f_i connect to v-nodes c_j only if h_{ij}=1.

2.2 LDPC Encoder

LDPC codes usually described by (N, K) notation, where N is the codeword length, K is the information length and N-K represent the redundant bits which added to the information block by the encoding process [9]. Every linear block code has a generator matrix G-matrix at the encoder and parity check matrix H-matrix at the decoder. In LDPC code the two matrices are interrelated. At the encoder the message is multiplied by G-matrix to get N bit codeword.

$G_{K*N} = [I_K \; P_{K*(N-K)}]$ ……. (1)

From H-matrix, G-matrix is derived

$H_{(N-K*N)} = [P^T I_{N-K}]$ …….. (2)

Where I is the identity matrix.

If the codeword is C, at the decoder the syndrome must equal to zero to satisfy that the codeword is error free [10].

At the encoder

$C = K * G$ ..…… (3)

At the decoder

$S = C * H^T$ ……. (4)

2.3 LDPC Decoder

LDPC code used the iterative decoding method (Message Passing Algorithm) on the tanner graph, where the variable node and check node exchange multiple messages until the parity check condition ($C*H^T = 0$) is satisfied.

The iteration process has two main algorithms [11], hard decision (Bit Flipping) decoding algorithm and Soft decision decoding algorithm.

2.3.1 Hard Decision (Bit Flipping) Decoding Algorith

In this algorithm, variable nodes send a message. Here is a binary message (0 or 1) to their connected check nodes then every c- node make mod2 process on the messages received from the v- nodes, if the result is zero, it will send the same v-nodes, v-nodes decide the bit value depending on the message received from c-nodes by the majority role. This process will stop if the parity check equation is satisfied or the number of iterations has passed its maximum value [12] [3].

2.3.2 Soft Decision (Sum-Product)

Soft decision message passing algorithm on the contrast of hard decision message passing algorithm, use the probability of the received bit and this probability represent the log likelihood ratio (LLR). The received bit probabilities before decoder running called Priori probabilities, while the probabilities received from the decoder called the posterior probabilities [13]. If we consider the variable is x, then P(x = 1) = 1−P(x = 0), which mean from P(x = 1) the probability of the P(x = 0) can be known, so there is a need to store one probability value for x. log likelihood ratios are used to represent the metrics for binary variable [14]. Where

$L(x) = \text{Log}\,(P\,(X=0)/P\,(X=1))$ ……. . (5)

3. MATLAB SIMULATION

Two types of LDPC code applications, DVB-S2 LDPC Code and WLAN802.11n LDPC code for different block lengths, code rates, and number of iterations, these codec are designed and simulated in MatLab

3.1 DVB_S2 LDPC Code Standard.

Digital Video Broadcasting-Second generation (DVB_S2). This standard has eleven code rates, 9/10, 8/9, 5/6, 4/5, 3/4, 2/3, 3/5, 1/2, 2/5, 1/3 and 1/4 [15]. Figure (2) shown below represents the model which consist of LDPC code as a channel coding method, BPSK modulation and the signal will be transmitted over an AWGN channel. Three code rates was used as mentioned in the table (1), only 1/4, 1/3, 1/2 were used and a comparison between of them in BER performance were done for different values of iteration.

Table (1): Simulation Parameters for DVB-S2 LDPC

Code rate(R)	Information bits (K)	o/p codeword
1/4	16200	64800
1/3	21600	64800
1/2	32400	64800

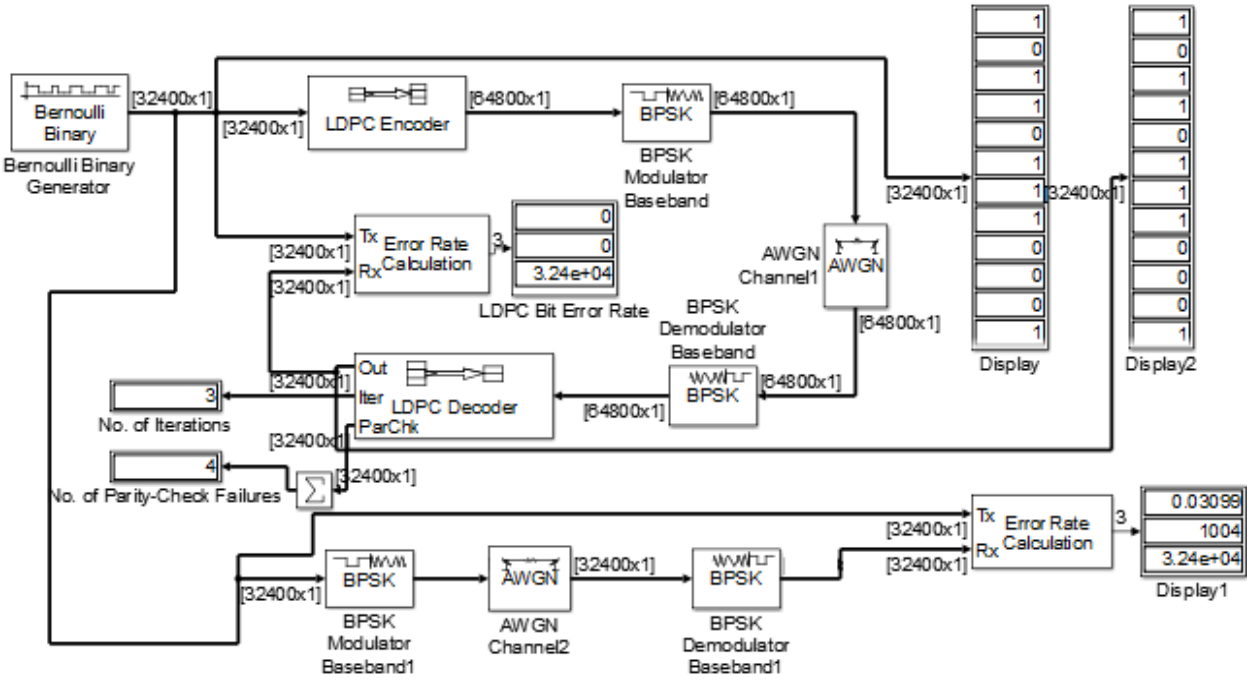

Figure (2): Simulink model for LDPC Code.

3.2 LDPC Code for IEEE802.11n

Another type of LDPC code called Quasi-Cyclic (QC-LDPC) code, it has an efficient performance, and it's used in modern wireless communication standards, as IEEE 802.11n, IEEE 802.11ac, and IEEE 802.16e [16]. Here efficient encoding used, where H-matrix used in the encoder instead of G-matrix as in [17]. And its parity check matrix consisting of Z × Z square sub-matrices, each one is an identity matrix with a cyclic shift or a null matrix [18]. These sub matrices are concatenated to compose twelve deferent matrices of length 648, 1296 and 1944 of 1/2, 2/3, 3/4 and 5/6 code rates [19]. In this paper only code rate 1/2 is used. Figure (3) shows the simulation model, where binary random signal is generated and encoded using efficient LDPC encoding using H-matrix instead of G-Matrix, the encoded signal modulated using BPSK modulation and sent via AWGN channel, the reverse process done at the receiver.

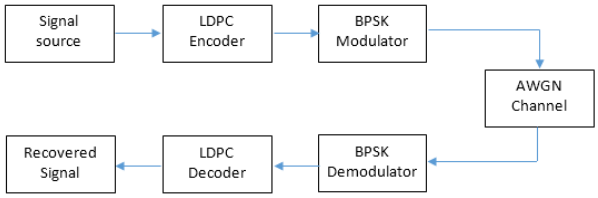

Figure (3): IEEE 802.11n LDPC Code Simulation.

One of matrices used for this type shown below. H-matrix of code rate =1/2, Z=81 andL_{cw} (codeword length) =1944 [20].

```
[57 -1  -1 -1 50 -1 11 -1 50 -1 79 -1 -1  0 -1 -1 -1 -1 -1 -1 -1 -1 -
 3  -1  28 -1  0 -1 -1 -1 55 7  -1 -1 -1  0  0 -1 -1 -1 -1 -1 -1 -1 -
30 -1  -1 -1 24 37 -1 -1 56 14 -1 -1 -1 -1  0  0 -1 -1 -1 -1 -1 -1 -
62 53  -1 -1 53 -1 -1 3  35 -1 -1 -1 -1 -1 -1  0  0 -1 -1 -1 -1 -1 -
40 -1  -1 20 66 -1 -1 22 28 -1 -1 -1 -1 -1 -1  0  0 -1 -1 -1 -1 -1 -
0  -1  -1 -1  8 -1 42 -1 50 -1 -1 8  -1 -1 -1 -1 -1  0  0 -1 -1 -1 -
69 79  79 -1 -1 -1 56 -1 52 -1 -1 -1  0 -1 -1 -1 -1 -1  0  0 -1 -1 -
65 -1  -1 -1 38 57 -1 -1 72 -1 27 -1 -1 -1 -1 -1 -1 -1 -1  0  0 -1 -
64 -1  -1 -1 14 52 -1 -1 30 -1 -1 32 -1 -1 -1 -1 -1 -1 -1  0  0 -1 -
-1 45  -1 70 0  -1 -1 -1 77 9  -1 -1 -1 -1 -1 -1 -1 -1 -1 -1  0  0 -
2  56  -1 57 35 -1 -1 -1 -1 -1 12 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1  0
24 -1  61 -1 60 -1 -1 27 51 -1 -1 16 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1
```

4. SIMULATION RESULTS

Simulation results of the two application types of LDPC code in different code rates, block lengths and different number of iterations will be explained.

For DVB-S2 LDPC code, as indicated by the results, BER decreases as the number of iterations increase (iteration the number of times the decoding process is repeated until the final decision is made) as shown in figure (4). And as the code rate decreases the BER performance will be better as noted in figure (5) the BER performance for R=1/4 is better than it for R= 1/3 and 1/2.

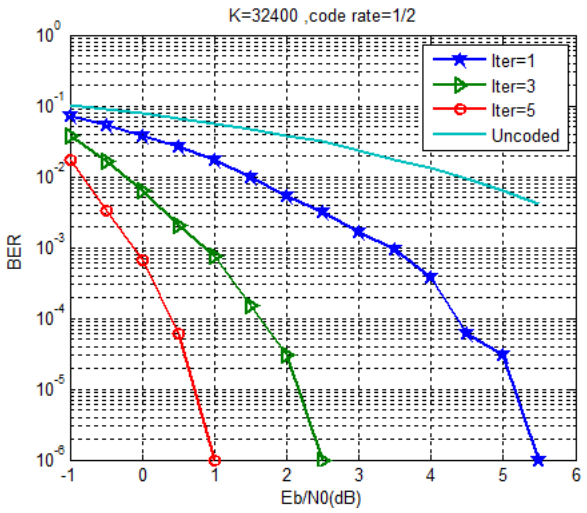

Figure (4): Figure Shows BER Performance with Different Iteration Values for K=32400 and Code Rate =1/2.

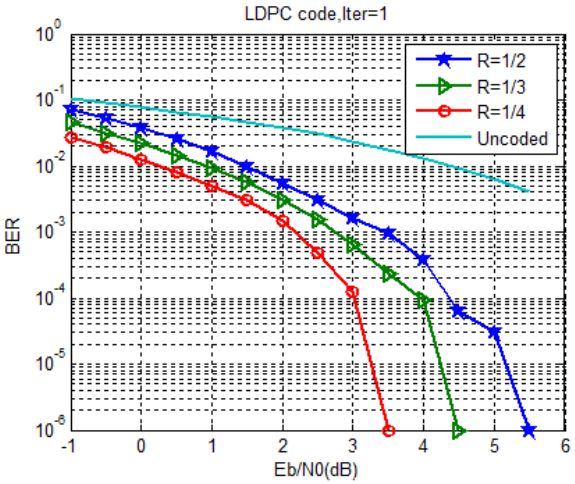

Figure (5): Figure Shows BER Performance with Different Code Rates in Iteration=1.

For 802.11n LDPC code, also note that the BER decreases with increasing the codeword length and with increasing the number of iterations. As shown in figures (6) and (7).

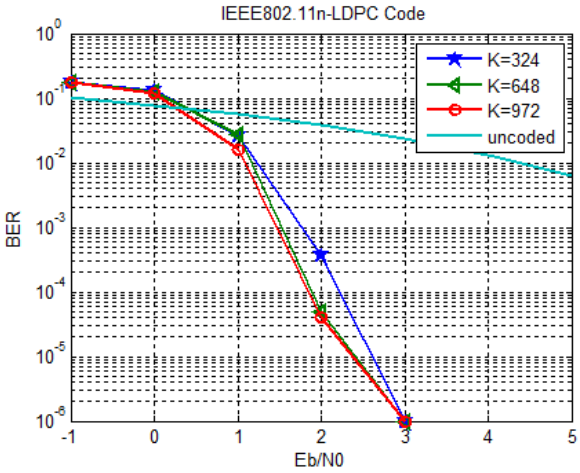

Figure (6): BER Performance for Different Block Lengths of Rate ½ LDPC Code.

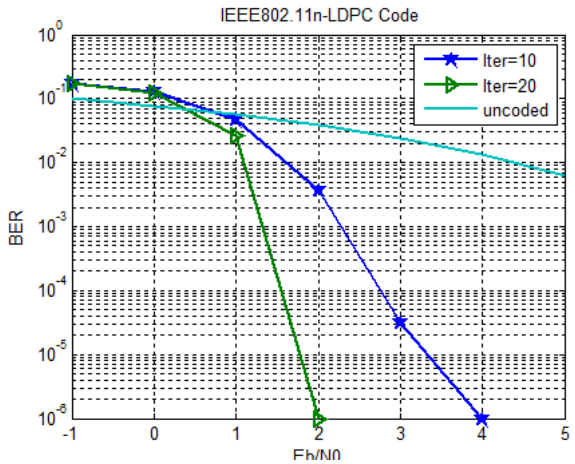

Figure (7): BER Performance for Different Iterations of K=648 of Rate ½ LDPC Code.

5. CONCLUSION

LDPC code represents a powerful error correction code, but its performance depends on its design and the choice of its parameters. As shown in results, DVB-S2 LDPC code has a better performance than IEEE802.11n LDPC code, especially at low Eb/N0 values. As shown in figure (4), DVB-S2 LDPC code of K=32400 of 1/2 code rate at iteration=5 achieved BER=10^{-6} at Eb/N0=1 dB, while, IEEE802.11n for K=648 of ½ code rate achieved BER= 10^{-6} at Eb/N0=2dB with iteration =20 as shown in figure (7). But, for two types the BER performance is good with respecting to the uncoded block performance and its performance will be better as the number of iterations increase.

6. REFERENCES

[1] K. Deergha Rao, Channel Coding Techniques for Wireless Communications, Springer India, 2015.

[2] BERNARD SKLAR, PABITRA KUMAR RAY, Digital Communications Fundamentals and Applications, second edition, 2014 Dorling Kindersley (India) Pvt. Ltd.

[3] Susmitha Remmanapudi, Balaji Bandaru , An FPGA Implementation Of Low Density Parity-Check Codes Construction & Decoding, International Conference on Devices, Circuits and Systems (ICDCS), pp. 216-220, 15-16 March 2012.

[4] SARAH J. JOHNSON, Iterative Error Correction Turbo, Low-Density Parity-Check and Repeat–Accumulate Codes, Cambridge University, 2010.

[5] Sukhleen Bindra Narang, Kunal Pubby and Hashneet Kaur," Low-density parity check (LDPC) codes: A new era in coding", Signal And Image Processing An International Journal SIPAIJ, Vol. 1, No. 1, 2016.

[6] Palleti Raju and Potnuru Surya Prasad, Design of an LDPC Decoder and Its Performance, International Journal of Electrical and Electronics communication Vol.1, No. 1, 2017.

[7] Swapnil Mhaske, Hojin Kee, Tai Ly, Ahsan Aziz and Predrag Spasojevic1, FPGA-Based Channel Coding Architectures for 5G WirelessUsing High-Level Synthesis**,** International Journal of Reconfigurable Computing, 2017.

[8] R. El Alami, C. B. Gueye, M. Boussetta, M. Zouak and M. Mrabti, Bit Flipping-Sum Product Algorithm for regular LDPC codes, 5th International Symposium On I/V Communications and Mobile Network, pp. 1-4, 2010.

[9] Seema S. Gumbade, Anirudhha S. Wagh and Dr.D.P.Rathod, REVIEW ON CONSTRUCTION OF PARITY CHECK MATRIX FOR LDPC CODE, International Journal of Recent Trends in Engineering & Research (IJRTER), Vol. 03, No. 04, April - 2017 **.**

[10] Pavel Straus and Zdenek Kolka, Simulation and Implementation of LDPC Code in FPGA", 23rd International Conference Radioelektronika (RADIOELEKTRONIKA), pp. 346 – 349, 16-17 April 2013.

[11] Rinu Jose and Ameenudeen Pe, Analysis of Hard Decision and Soft Decision Decoding Algorithms of LDPC Codes in AWGN", IEEE International Advance Computing Conference (IACC), pp. 430 – 435, 2015.

[12] Sarah J. Johnson, Introducing Low-Density Parity-Check Codes, School of Electrical Engineering and

Computer Science, the University of Newcastle, Australia, May 2010.

[13] Er. Sonia and Er. Swati Gupta, Hard Decision and Soft Decision Decoding Algorithms for LDPC and Qc-LDPC Codes, International Journal of Computer Applications (IJCSMC), Vol. 4, No. 9, pp. 182-191, September 2015**.**

[14] Namrata P. Bhavsar and Brijesh Vala , Design of Hard and Soft Decision Decoding Algorithms of LDPC, International Journal of Computer Applications (0975 – 8887), Vol. 90, No. 16, March 2014.

[15] Bačić Iva et al," DVB-S2 Model Based on Reed-Solomon Outer Encoder", IARIA, 2012.

[16] Monica Mankar, Gajendra Asutkar and Pravin Dakhole, Reduced Complexity Quasi-Cyclic LDPC Encoder For IEEE 802.11N, International Journal of VLSI design & Communication Systems (VLSICS), Vol.7, No.5/6, December 2016.

[17] Thomas J. Richardson, Rüdiger L. Urbanke, Efficient Encoding of Low-Density Parity-Check Codes, IEEE Transactions On Information Theory, VOL. 47, NO. 2, pp. 638-656, FEBRUARY 2001.

[18] Yong-Min Jung1, Chul-Ho Chung1, Yun-Ho Jung2, and Jae-Seok Kim1,7.7 Gbps Encoder Design for IEEE 802.11ac QC-LDPC Codes, Journal Of Semiconductor Technology And Science, VOL.14, NO.4, pp. 215-218, AUGUST, 2014.

[19] Merve Peyic, Hakan Baba, Erdem Guleyuboglu, Ilker Hamzaoglu and Mehmet Keskinoz, A low power multi-rate decoder hardware for IEEE 802.11n LDPC codes, Microprocessors and Microsystems, Vol. 36, No. 3, pp. 159-166, 2012.

[20] Swapnil Mhaske, High-Throughput FPGA QC-LDPC Decoder Architecture for 5G Wireless, Master of Science Graduate Program in Electrical and Computer Engineering Graduate School, New Brunswick Rutgers, The State University of New Jersey, October 2015.