Low Power High Speed for LCD Flat Panel Display Application

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ABSTRACT

A low power buffer amplifier for LCD panel driving system is presented. The proposed architecture has self-biased RAIL TO RAIL complementary differential pair for full input output swing, and class B push-pull output driving stage which is suitable for large and small size liquid crystal display, compensation capacitor and resistance are used to improve the settling time and slew rate of the buffer amplifier by stabilizing phase margin, an experimental prototype is simulated using cadence specter in .35 µm CMOS technology which draws only 8 µm static current and provide a settling time of 2.8 µs and rising and 3 µs during four the act area for the design of the buffer is 49*60 µm With power supply of 3.3 it with stand with 1000 pF load capacitance the power consumption of the amplifier under static condition is 66µW.

Keywords

Rail Operational Amplifier

1. INTRODUCTION

With increasing demand of high speed low power liquid crystal display in recent years, we have to match with these requirements to consummate the market demand. LCD driver generally contains shift registers, input register's, data latch, level shifter , digital to analog converter, Pre-Emphasis, and analog buffers the output buffer amplifier is vigorously affects the speed, resolution, voltage swing and power dissipation [12],[4],[8],[9]. For each pixel we a buffer amplifier is required so as the number of pixel increases the number of buffers on the panel to drive increases, nowadays battery operated portable devices are acclimated to increase the performance and to elongate the battery life we require low-power high-speed buffer amplifier LCD output buffer amplifier are realized by operational amplifier in unity gain configuration generally RAIL TO RAIL operational amplifiers are acclimated to get plenary output swing RAIL TO RAIL operation amplifiers are consist of complimentary differential amplifiers at first stage and a summing current source at second is stage with generally kenned as folded cascaded architecture then the output is stage which are this work in class B and class AB push pull stage.

2. PROPOSED BUFFER DRIVING SCHEME

Generally introducing zero in transfer function of buffer amplifier using phase compensation register & output load Capacitance it makes the buffer stable but the slew rate is limited as due to small slew rate the settling time for large

A typical two stage operational amplifier requires compensation for the stability some buffer amplifier's takes the output node as the dominant to achieve the stability without Miller capacitance[3,6] however charge conservation technique is commonly used in some LCD driver to reduce the dynamic power dissipation[1,2]

3. ZERO COMPENSATION TECHNIQUE

Zero compensation technique is generally used to get the dominant pole in buffer amplifier figure 1 shows a buffer amplifier with zero compensation. And fig 2 shows the configuration of proposed buffer amplifier using zero compensation technique. Fig 4 shows the schematic of proposed buffer amplifier

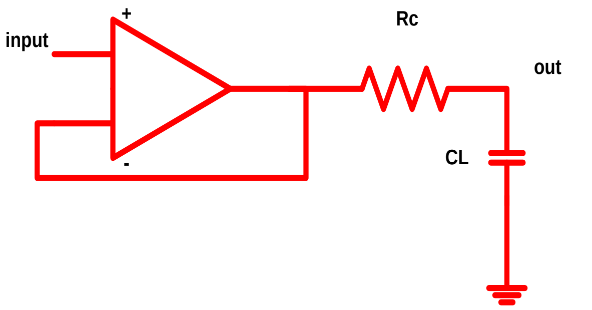

Fig 1: zero compensation buffer amplifiers

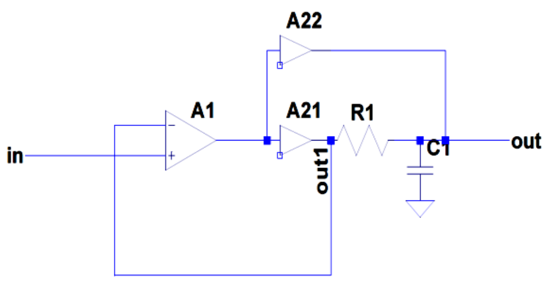

Fig 2: Configuration of proposed buffer.

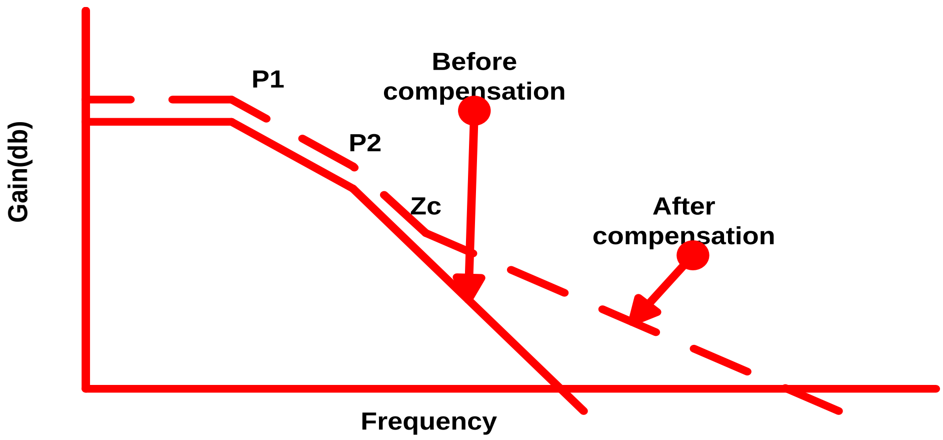

Fig 3: Frequency response of buffer amplifier

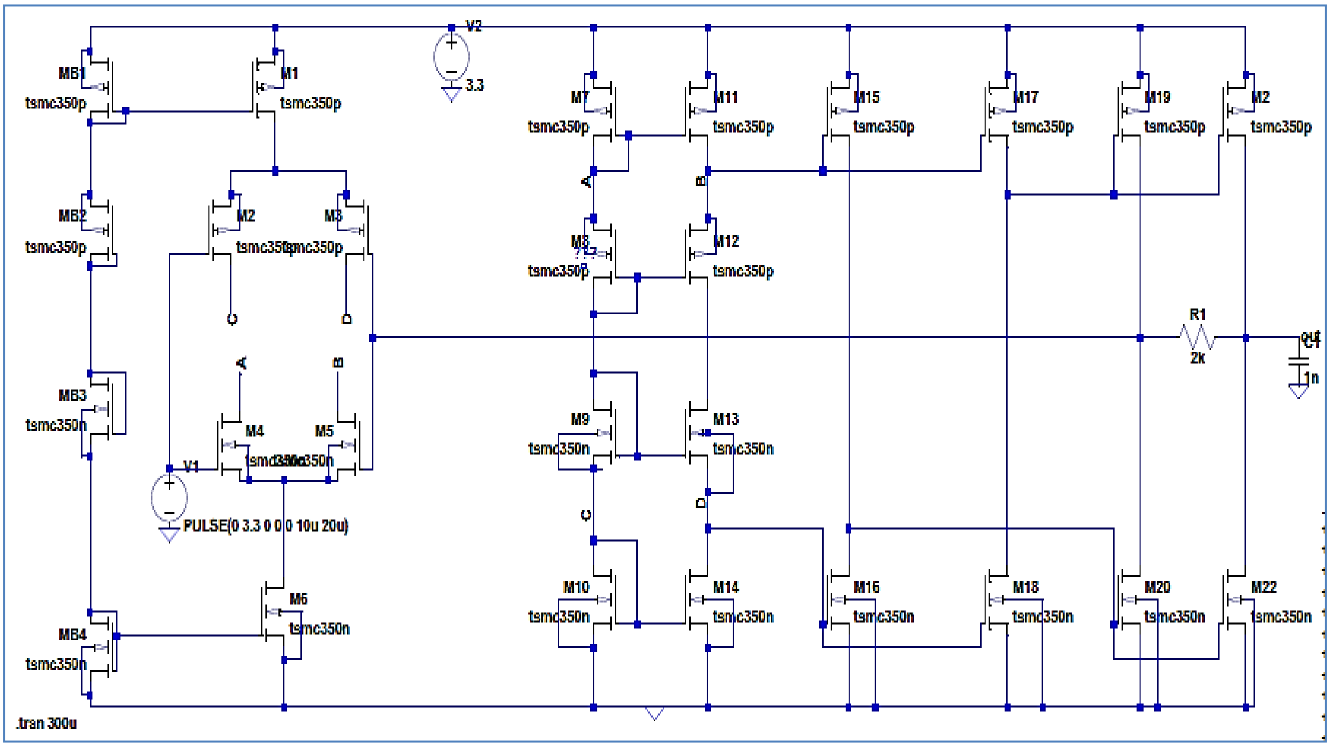

Fig 4: Schematic of proposed buffer amplifier

In figure 3 solid line shows frequency characteristic before compensation and dotted line after compensation, As dominant pole P1 shifted towards origin as with increasing load capacitance means gain bandwidth will decrease it also makes system unstable and degrade phase margin, for proper operation of buffer for high speed phase margin should be in between 70° to 45° generally they prefer 60° phase margin for high speed low-power buffer amplifier design here using "$R_C C_L$" introduces required phase margin, it introduce a zero in transfer function.

$$Z_C = \frac{-1}{R_C C_L} \qquad \ldots (i)$$

This is called as zero compensation technique for large phase margin, it is generally used when we does not use them Miller capacitor in between differential amplifier and output is stage of differentiated amplifier. The value of zero located to left the most of unity gain bandwidth to the college RGB

$$\zeta = R_C \sqrt{C_L} \qquad \ldots (ii)$$

For 70° phase and margin $\zeta \geq 1$ and amplifier is stable, for $\zeta < .6$the phase margin is approximately given as I moved to women in

PM $\approx 100 \times \zeta \;..(iii)$ and settling time = $\frac{4}{\zeta \omega_n}..(iv)$

To get large phase margin R_C should be large but we can't increase the resistance R_C, so much as it decreases the settling time, so there is compromise in between phase margin and settling time to get optimum phase margin. As to account large capacitive load we have to increase the biasing current but it will increase the power loss in buffer amplifier, to solve on the issue to account the large capacitive load current dynamic current sensing technique is used to provide extra biasing current only during transition of input signal with the help of voltage divider method the current sensing technique sense the falling and rising edge according to that it provide the extra biasing current.

4. SMALL SIGNAL ANALYSIS OF PROPOSED

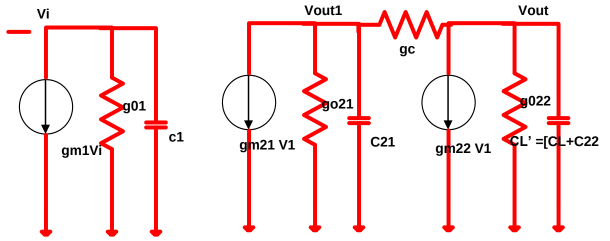

Fig 5: Small signal model of proposed buffer.

The small signal of the proposed driving scheme is shown in figure 5 when we does not count the the transconductance of complimentary differential pair is gm1, and gm21,gm22 are the transconductance of two competitors, and g01,g021 and g022 are the output conductance, and C_1, C_{21} *and* C_{22} are the paracetic capacitance.

The open loop transfer function of the buffer ,

$$A_0(s) = \frac{V_{out1}(s)}{V_i(s)} \approx A_{dc}\frac{\left(1-\frac{s}{Z_c}\right)}{\left(1-\frac{s}{P_1}\right)\left(1-\frac{s}{P_2}\right)} \quad \dots(v)$$

where

$$A_{dc} = \frac{g_{m1}(g_{m21}g_C + g_{m21}g_{022} + g_{m22}g_C)}{g_{01}(g_C g_{021} + g_C g_{022} + g_{021}g_{022})}$$

$$\approx \frac{g_{m1}(g_{m2} + g_{m22})}{g_{01}(g_{021} + g_{022})} \quad \dots(vi)$$

$$P_1 = -\frac{(g_C g_{021} + g_C g_{022} + g_{021}g_{022})}{C'_L(g_{021} + g_C)}$$

$$\approx \frac{g_{021} + g_{022}}{C'_L} \quad \dots(vii)$$

$$P_2 = -\frac{g_{01}}{C_1} \quad \dots(viii)$$

$$Z_C = -\frac{(g_{m21}g_C + g_{m21}g_{022} + g_{m22}g_C)}{C'_L g_{m21}} \quad \dots(ix)$$

The above Equivalent circuit contains three poles and zero the third pole is far away from other poles and zero, so it is neglected, g01,g021 and g022 conductance are much smaller than gc, the parasitic capacitance is also much smaller than load capacitance these aproximations are taken for the analysis.

The closed loop transfer functiom of buffer,

$$A_{c1}(S) = \left(\frac{V_{out1}(s)}{V_i(s)}\right)_{closed\ loop} = \frac{A_{01}(s)}{1 + A_{01}(s)}$$

$$\approx \frac{\left(1-\frac{s}{Z_c}\right)}{1 - s\left(\frac{1}{AP_1} + \frac{1}{Z_C}\right) + s^2\frac{1}{AP_1P_2}} \quad \dots(x)$$

the relation between Vout1 and Vout2 from the figure 5 is expressed as:

$$\frac{V_{out}}{V_{out1}} \approx \frac{1 + S\frac{g_{m22}C_{21}}{g_{m21}g_C + g_{m22}g_C + g_{m22}g_{o21}}}{1 + S\frac{g_{m21}C_L}{g_{m21}g_C + g_{m21}g_{022} + g_{m22}g_C}} \quad \dots(xi)$$

the closed loop transfer function of overall block as shown in figure 4:

$$A_c(S) = \left(\frac{V_{out1}(s)}{V_i(s)}\frac{V_{out}(s)}{V_{out1}(s)}\right)_{closed\ loop}$$

$$= \frac{1 + S\frac{g_{m22}C_{21}}{g_{m21}g_C + g_{m22}g_C + g_{m22}g_{o21}}}{1 - s\left(\frac{1}{AP_1} + \frac{1}{Z_C}\right) + s^2\frac{1}{AP_1P_2}} \quad \dots(xii)$$

The zero from the data transfer function is neglected as it is far away from the dominant pole.

$$A_c(S) \approx \frac{1}{1 - s\left(\frac{1}{AP_1} + \frac{1}{Z_C}\right) + s^2\frac{1}{AP_1P_2}} \quad \dots(xiii)$$

and it is equivalent to second o order transfer function so,

$$\omega_n = \sqrt{A_{dc}P_1P_2} \quad \dots(xiv)$$

$$\zeta = -\frac{1}{2}\sqrt{A_{dc}P_1P_2}\left(\frac{1}{A_{dc}P_1} + \frac{1}{Z_C}\right) \quad \dots(xv)$$

$$\zeta \approx \frac{g_{m21}R_C}{2}\sqrt{\frac{g_{m1}C_L}{(g_{m21} + g_{m22})C_1}} \quad \dots(xvi)$$

As from the above expressions damping factor ζ depends upon transconductance gm1, and the resistance of MOS using the push-pull output is stage depends upon the current flowing and push-pull stage With the use of dynamic bias sensor , we increase the biasing current during the transition phase of input this results in increase of transconductance gm1 and decreasing output resistance of push-pull stage during charging and discharging with load capacitance, as the settling time depends upon damping factor and natural frequency both this parameters increases with increasing transconductance of gm1 where gm1 is the transconductance of differential is stage, this results and decreasing the settling time means the response of buffer amplifier increases with the use of dynamic bias sensor.

5. DESIGN PARAMETERS OF RAIL-RAIL OPERATIONAL AMPLIFIER

Table 1: Design parameters of rail-rail operational amplifier

S. No.	PARAMETERS	VALUE
1.	Process	.35 µm CMOS technology
2.	Power supply	3.3 V
3.	Load resistance	20 kΩ
4.	Load capacitance	1000 pF
5.	Power dissipation	1mW
6.	DC gain	95 db
7.	Gain bandwidth product	1 MH
8.	Phase margin	70°
9.	Slew rate	5 V/ µs
10.	Output voltage swing	0-3.3 V
11.	Input common mode range	0-3.3 V
12.	Output stage	Class B

6. SIMULATION RESULT

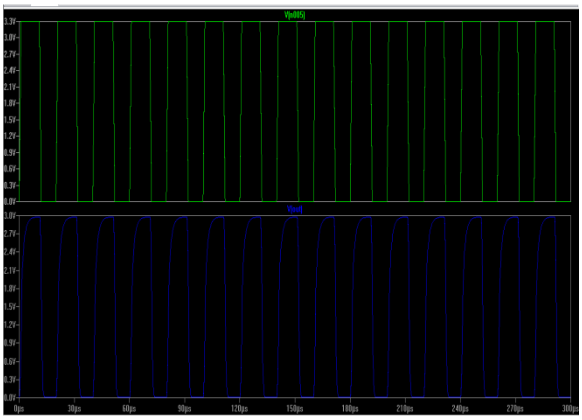

Fig 6: Simulation result for step response.

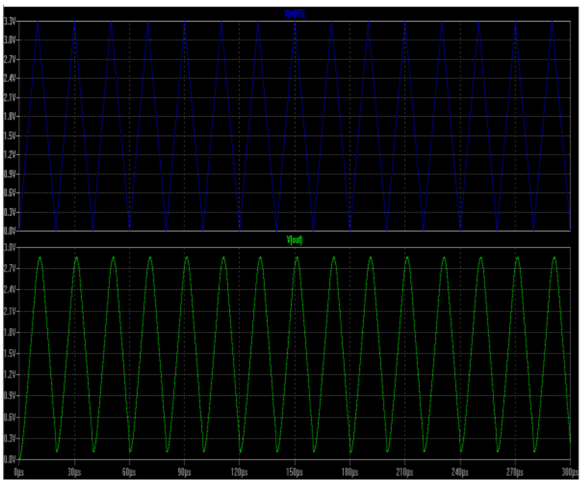

Fig 7: Simulation result for triangular response.

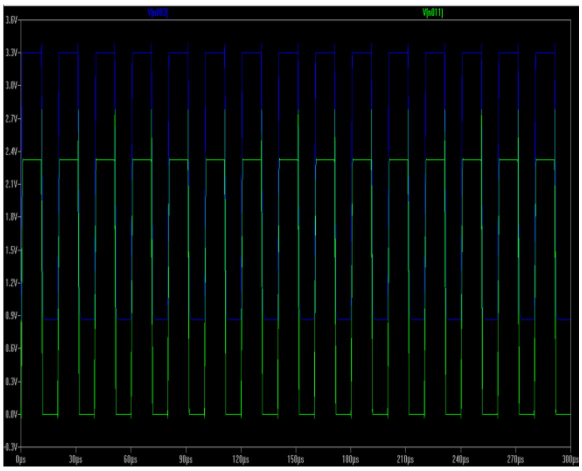

Fig 8: Current at trail end of PMOS & NMOS differential pair.

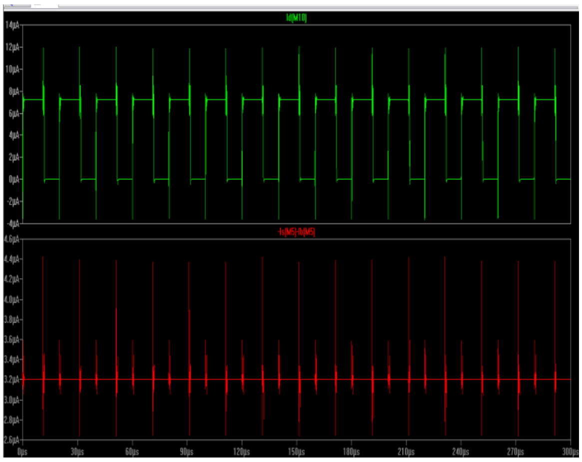

Fig 10: Static current in biasing network and differential pair.

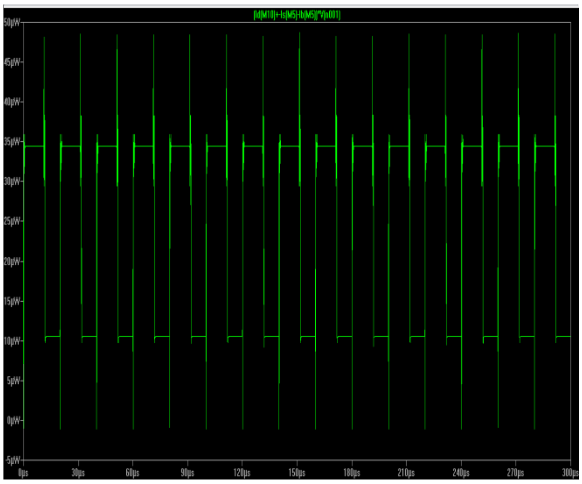

Fig 9: Power consumption differential pair during static condition.

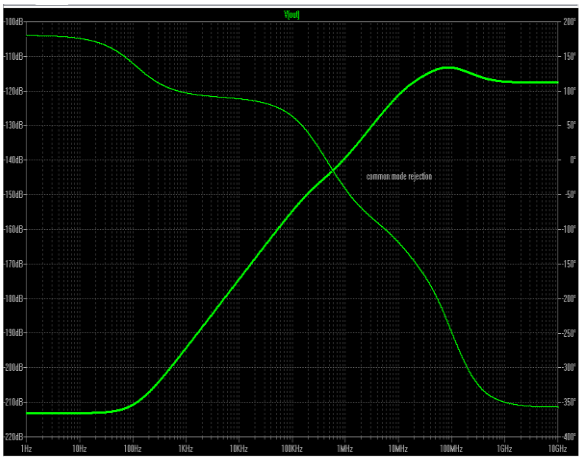

Fig 11: simulation result of common mode rejection ratio.

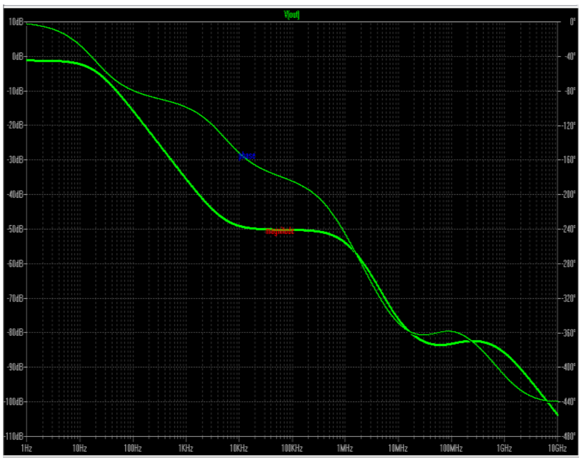

Fig 11: Frequency response of proposed buffer amplifier.

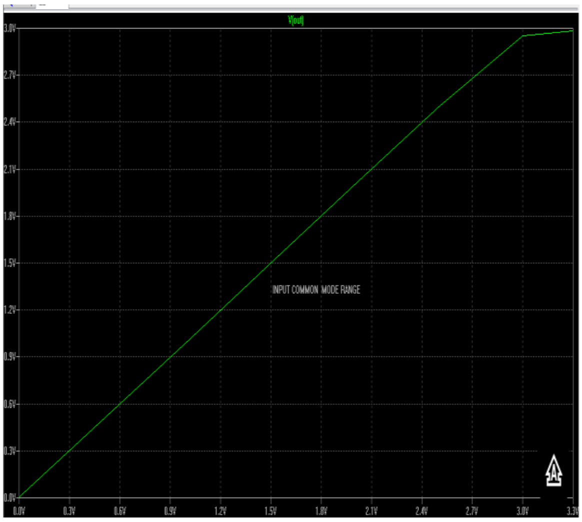

Fig 12: Simulation result of Input common mode range.

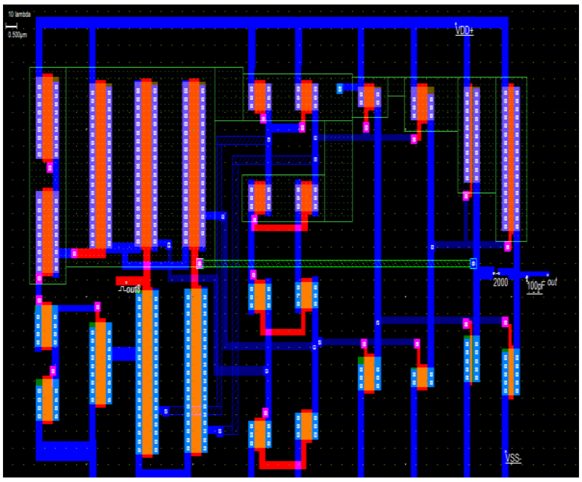

Fig 13: Layout diagram of rail to rail differential amplifier.

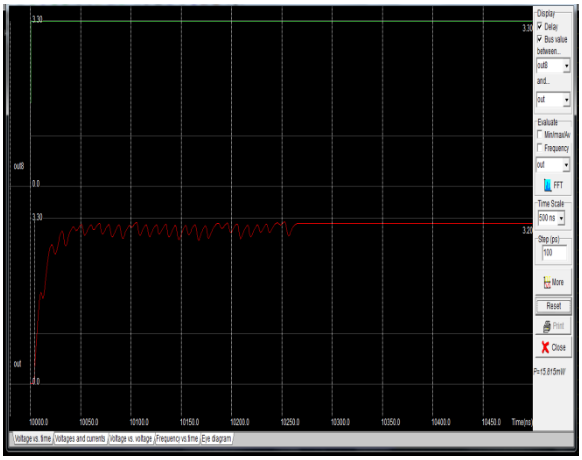

Fig 14: Simulation result of differential amplifier for step response.

7. COMPARISON TABLE

Table 2: Comparison Table

	Ref [20]	Ref [3]	Ref.[4]	Ref.[1]	This work is
CMOS technology (μm)	.6	.6	.6	.5	.35
Supply voltage	5V	5 V	5 V	5 V	.33 V
Max load capacitor	680 pF	170 pF	30 pF	1000 pF	1000 pF
Quiescent current	30 μA	5 μA	8.2 μA	32 μA	8 μA
Power	150 μW	75 μW	150 μW	160 μW	66 μW
Settling time	1.2 μs	9.6 μs	8.2 μs	.7 μs	3.2 μs
Input-output range [V]	.15/4 V	.15/4.8V	.5/4.5 V	0/5 V	0/3.2 V
Input-output range [VDD%]	77%	93%	80%	100 %	97 %
Slew rate	–	–	–	–	7 V / μs
Active area [μm²]	**N/A**	**N/A**	**N/A**	**73 × 91**	**50 ×60**

8. CONCLUSION

Self-biased high-speed low-power rail to rail buffer amplifier for LCD is proposed work under class B operation which is suitable for small and large size LCD panel, the Zero compensation is used to enhance the slew rate and settling time the compensation resistor value should be optimized to get the optimal value of slew rate and phase margin, as with large value of compensation resistor we get adequate phase margin but it will increase settling time and vice versa. A prototype of this buffer is implemented on .35 μm CMOS technology it draws only is 8 μA static current. The buffer draws little static current but has a large driving capability during transition phase , full swing is obtained by RAIL TO RAIL operational amplifier and enlarge driving capability is obtained by the use of two comparators. The buffer is 3 μs of rising settling time and 3.2 μs of falling settling time, the active area occupied by the buffer is approximately 3600 μm². The performance of the proposed buffer is compared with previous buffer it is superior in power consumption, low static current and small settling time.

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