Abstract

The measurement of electrical activity of the heart via electrodes is named as Electrocardiography (ECG). An efficient compression technique using the compressive sensing method is required. Compressive Sensing (CS) holds the promise to be a key for acquisition and reconstruction of sparse signals. The reconstruction of such signals makes sampling rates below Nyquist rate. In this work, a novel framework was proposed that is based on the idea of CS theory for the compression of mother and fetal heart beats. The proposed scheme is based on the sparse representation of the components derived from the curvelet transform of the original Electrocardiogram (ECG) signal. The ECG signals may be approximated by a few coefficients that can be taken from a wavelet basis. This fact allows a compressed sensing approach for ECG signal compression to be introduced and to be a domain of search. ECG signals illustrate redundancy between adjacent heart beats. This redundancy implies a high fraction of common support between consecutive heart beats. The main contribution of this paper lies in the using of curvelet transform in order to generate sparsity in ECG signal. This transformation is considered an excellent approach as illustrated in this paper. Simulation
results represent a better approach than Discrete Wavelet Transform (DWT) that is based on compression of ECG. MIT-BIH database is used for experimentation. The MIT-BIH database contains different kinds of ECG signals that include both abnormal ECG and normal ECG, which have different sampling rates. MATLAB tool is used for simulation purpose. The novelty of the method is that the Compression Ratio (CR) achieved by detail coefficients is better. The performance measure of the reconstructed signal is carried out by Percentage Root Mean Difference (PRD). This paper also introduces the efficient realization of the different transformation techniques using FPGA. Thus the contribution of this paper lies into two main parts. The first part is specialized in determining the proper transformation that is used in the compression of ECG signals. The second part of the contribution is summarized in using suitable hardware to implement this design. Architecture can be based on the ideas of parallelism and pipelining to get the minimum throughput and speed. Architecture is cascade and simple for calculating curvelet coefficients. The reduction of the memory size can be done by splitting ROM table. The description and functionalities of the design are modeled by Verilog HDL. The simulation and synthesis methodology are used on Virtex-II Pro FPGA that uses less number of resources of the FPGA.

References


Index Terms

Computer Science
Signal Processing

Keywords

Compressive sensing; Sparse; Sampling rates; Heart beats; Compression ratio; FPGA