Abstract

This paper proposes a design of an asynchronous switch interfacing circuit between any numbers of different local clock synchronous domains. The asynchronous switch will generate a slower clock frequency from different local clock modules and moderate the high rated clock domain to slow down its clock frequency without stopping or pausing any clock of them during the data communication phase. The proposed design is implemented using the CMOS 45nm technology of STMicroelectronics and simulated using timed VHDL model (Xilinx ISE Design Suite 12.1). The delay time is required to change the clock frequency is mathematically modeled. It is shown that the switching delay time depends on the number of multipoint communicating domains. The proposed system is designed to use a small number of circuit elements that results in conspicuous improvements in terms of power consumption, throughput, and circuit area.
Design of an Asynchronous Switch for Clock Domain Crossing Interfaces

References

17. A. Winstanley and M. R. Greenstreet, “Temporal Properties of self timed rings”,
Design of an Asynchronous Switch for Clock Domain Crossing Interfaces


Index Terms

Computer Science Circuits and Systems

Keywords

Switch, Local Clock, Asynchronous, multipoint, circuit area