Abstract

In this paper, the incorporation of pseudo-exhaustive built-in self-test capabilities into the boundary scan (BS) architecture is presented. The Boundary Scan Register (BSR) input cells are configured as a test pattern generator (TPG), and the BSR input and output cells are configured as a test response compactor (TRC) in the BIST mode. Instructions for both BS and BIST process are proposed that enable the test access port controller (TAPC) to control the BS and BIST process. The presented design supports the BIST of the target chip for both the cascaded and non-cascaded input and output cells of the BSR. In the register transfer level (RTL), the insertion of segmentation cells in the case of pseudo-exhaustive testing (PET) may affect the system timing due to the unequal sequential depth in the BIST mode, so it is required to insert delay flip-flops which add significant area overhead and degrade circuit performance. In addition, transferring every flip-flop into BIST flip-flop adds area overhead and degrades circuit performance in the normal mode of the chip. To compensate these problems, a proposed design that converts the presented sequential block into the combinational block (combinational equivalent). The incorporation of BIST capabilities into the boundary scan architecture with this
solution is presented. Finally, a complete example for BIST (Built-In Self-Test) boundary scan architecture and 16-bit parallel-pipelined multiplier as the CUT is presented. The simulation and design download are presented on the field programmable gate array (FPGA) chip. The hardware implementation using the interfacing through the personal computer as a master controller controls the test circuitry from the TAPC as a slave controller.

References


Index Terms

Computer Science

System Architecture

Keywords

Built-In Self-Test (BIST), Testing of digital circuits, Boundary scan, Design for testability, BIST for boundary scan, Pseudo-exhaustive testing.