Partial Adiabatic Logic

Abstract

As the semiconductor industries is in progress which follows Gordon Moore’s, Moore’s law faithfully from the past five decades. Also, with integrating more number of transistors along with the functional circuits in a single chip with new process technologies [4]. Thus, with the increasing growth in VLSI technologies, per chip area the transistors number of counts is also constantly increasing, but with the same rate the chips gate switching energies does not decrease, thus the heat removal becomes more difficult with the power dissipation rise and even more costly [1]. The cost of that of total power consumption can be reduced with the advancement in the transistor process technology. As we know that power dissipation and a propagation delay are the fundamental building blocks in any digital hardware [6]. Hence limiting the power dissipation through adiabatic operation promises reduction of power consumption largely [1]. In VLSI, the adiabatic logic circuits are one of the promising low power techniques which gives low power dissipation with an expense of delay [6]. At first, the adiabatic logic circuits working principle are discussed. Next, the adiabatic switching and how it can conserve power is discussed. This report also tells about different types of adiabatic logic families and its
classification as fully and partially adiabatic logics. This paper review also covers some of the important future research directions [1]. An emulative investigation is carried out on the proposed circuit in CADANCE tool at GPDK180nm technology node. Comparison has shown that it significantly saves power up to an extent of about a 70% of a proposed technique as compared to that of a conventional CMOS logic circuits within a transition frequency range of about 10 to 150MHz. The low power digital devices that is operated with a low frequency have strongly accepted the importance and the use of the emulation results obtained from this type of adiabatic logic circuits technique. Hence, a tiny circuit design, a high speed and an economical VLSI (Very Large Scale of Integration) circuits with low power dissipation of numerous circuits used today with this progress [4]. The present work proposes positive feedback adiabatic logics (PFAL) based Full-adder designs and is compared with the conventional CMOS circuit designs.

References


Index Terms

Computer Science
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Keywords

Adiabatic logic, conventional CMOS logic circuit and PFAL logic circuit.