Abstract

The MAC architecture of Vedic multiplier with ‘Urdhva-tiryakbhyam’ methodology for 16 bit MAC using Vedic multiplier is proposed. Equations for each bit of 32 bit resultant are calculated distinctly. They are chosen as they decrease vertical critical delay in comparison to the conventional architectures of MAC implemented using half adders only and so make the multiplier fast. The designs are coded in Verilog HDL and synthesized with Xilinx ISE 14.6 using virtex series of FPGA (Field Programmable Gate Array). The combinational delay calculated for proposed 16 × 16 bit multiplier is 10.50 ns. Further speed comparisons of compressor adders with traditional ones and proposed multiplier with popular methods for multiplication are shown. Results clearly indicate the better speed performance of our proposed Vedic multiplier

References


Index Terms

Computer Science
Circuits and Systems

Keywords

Multiply and Accumulate, Vedic Multiplier, Verilog HDL, half adder.