Design and Implementation of Power and Area Efficient 3-Bit Flash ADC using GDI Technique

Neetika Yadav
ECE Department
ASET, Delhi

Preeti Kumari
Department of VLSI
CDAC, Noida

ABSTRACT
ADC (Analog to Digital Converter) is a device which converts analog values into digital numbers; analog values usually are in the form of voltages. Flash ADC, also called parallel ADC, is used where maximum sampling rate is required. Although this is the fastest ADC but its main disadvantage is that it consumes a lot of area and also dissipates a large amount of power because it is formed of a series of comparators which are connected with priority encoder. In this paper to overcome these disadvantages, the number of comparators are reduced by using multiplexers to generate the reference voltage which are designed with a new technique called GDI and by using this,a 3 bit flash ADC is designed by completely modifying the analog and digital parts. This architecture is then compared with the CMOS based ADC and TG based ADC. This architecture uses only 3 comparators for a 3 bit ADC. This 3-bit ADC is designed and simulated in Mentor Graphics Pyxis schematic tool with 1.8 V supply voltage and 180 nanometer technology.

General Terms
Analog to digital converter, Gate Diffusion Input

Keywords
MUX,TG,GDI,ADC,DAC

1. INTRODUCTION
ADCs (Analog to Digital Converter) and DACs (Digital to Analog Converter) have become an integral part of any electronic system where the conversion from analog to digital domain and vice versa has become essential. ADC, which is an essential interface block for many systems, is a device used to convert a continuous physical signal usually in the form of voltage into digital numbers. There are various applications like optical communication, electronic test equipment, radar detection etc in which flash ADC is the choice of designers. Flash or Parallel convertors have the highest speed of any type of ADC.A N-bit flash ADC uses one comparator for each transition level ($2^N - 1$) and 2^N resistors, the reference voltage is divided into 2^N values, each of which is fed into a comparator. As shown in the figure 1, the input voltage is compared with each reference voltage and results in a thermometer code at the output of the comparators. The thermometer code shows all 0's for each resistor string input where V_{in} is less than the divided reference voltage at that resistor .

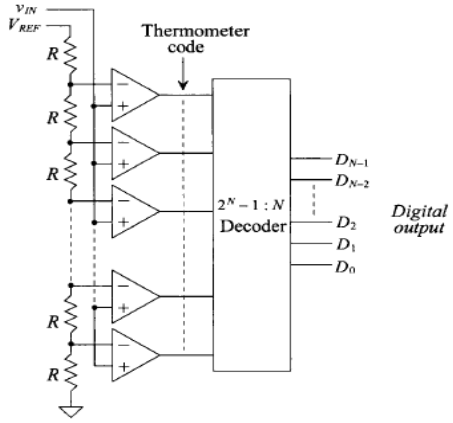

Fig.1: Architecture of Flash ADC

In this paper, two new architectures of flash ADC are proposed in which the number of comparators is reduced by using multiplexers to generate the reference voltage [1] which are designed with a new technique called GDI technique and comparator is basically designed with CMOS technique and in the second approach MUX is designed using transmission gate technique.

GDI technique uses two transistors where gates of both transistors are diffused together to form a single input hence the name Gate Diffusion Input. The basic GDI cell is shown in figure 2 in which ports P, G and N act as inputs and port out acts as output.

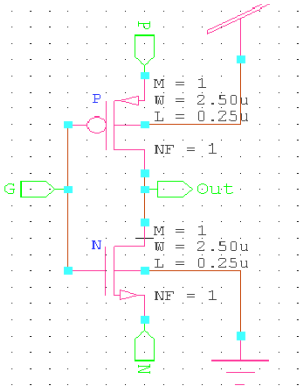

Fig.2: Basic GDI cell

Different outputs can be obtained by applying different values at the inputs of the basic GDI cell. The same GDI cell can work as MUX, AND, OR gate etc. Table 1 shows different possible outcomes for different inputs applied.

Table 1. Functional definition of basic GDI cell

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	INV
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX

Rest of the paper is organized as follows: in section II the conventional architecture of Flash ADC is shown followed by the architecture of the proposed technique in section III. In the section IV simulation results are given and the work is concluded in section V.

2. CONVENTIONAL ARCHITECTURE OF FLASH ADC

A typical architecture of conventional CMOS based Flash ADC is shown in figure 3, it consists of comparators and resistors to generate the reference voltage.

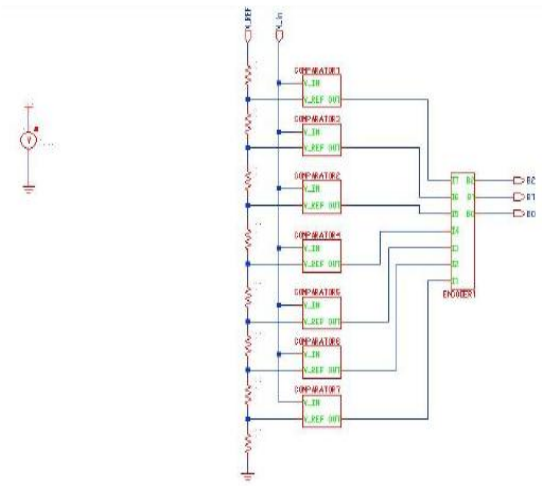

Fig.3: Schematic of CMOS based Flash ADC

In the conventional CMOS based ADC, the number of comparators and the resistors used are given by (2n-1) and (2n) respectively. The reference voltage supplied to each comparator is given as Vref(i/2^n) where ‘i’ is the number of resistors and ‘n’ being the number of bits of the input data. Each reference voltage is then compared with the input voltage which appears as the output of the comparators. The output comes out to be ‘0’ for each resistor string when input voltage is less than the divided reference voltage and ‘1’ when the input voltage is greater than the divided reference voltage. Then a simple 2n-1: n encoder is used to convert the compared data into n bit digital word.

3. PROPOSED FLASH ADC DESIGN

Architecture of proposed technique is shown in figure 4 in which number of comparators are reduced and MUX are used to generate reference voltage. The MUX used in first approach is made using transmission gates and for the second approach, MUX is designed using GDI Technique. The output of comparator1 is the MSB of the final output of ADC i.e. B2 and also works as the select line for 2x1 MUX whose output is fed at the negative terminal of the next comparator thus acting as the reference voltage. The output of comparator2 is the next bit of final output and denoted as B1 .Both B2 and B1 work as select lines for the next 4x1 MUX and this process is continued.

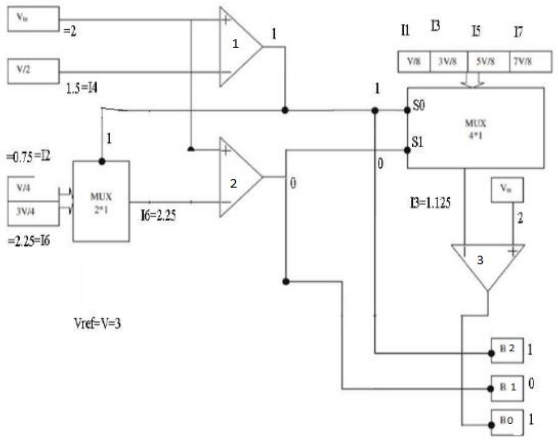

Fig.4: Proposed architecture

Schematic of proposed approaches i.e. Flash ADC using Transmission Gate and Flash ADC using Gate Diffusion Input (GDI) Technique are shown in the figure 5. The MUX used for these architectures is designed by using transmission gate (T.G) and G.D.I technique respectively.

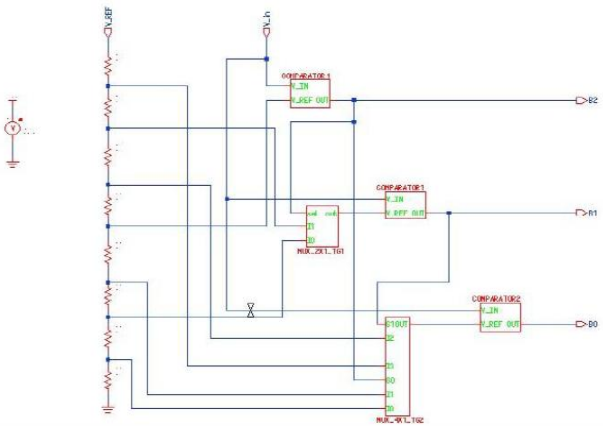

Fig.5: Schematic of proposed technique

The schematic of 2*1 MUX using TG is shown in figure 6, whose functionality is same as that of a MUX using CMOS.

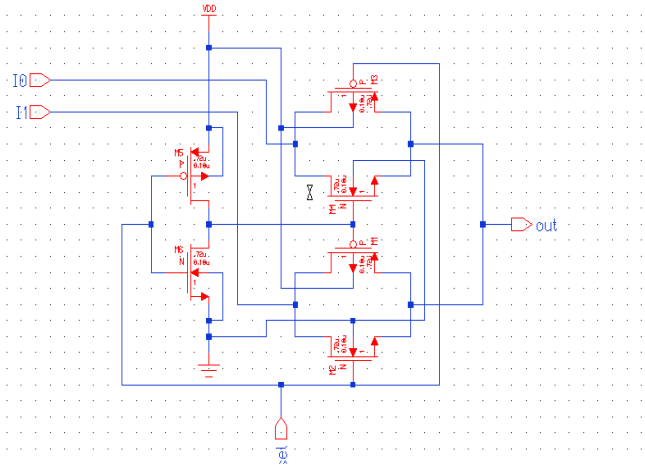

Fig.6: 2*1 MUX using TG

The 2*1 MUX using GDI Technique can be obtained by applying C at N, B at P, and A at G in fig.2 of the basic GDI

cell.

4. SIMULATION RESULTS

The simulation results of conventional architecture using CMOS is shown in figure 7.

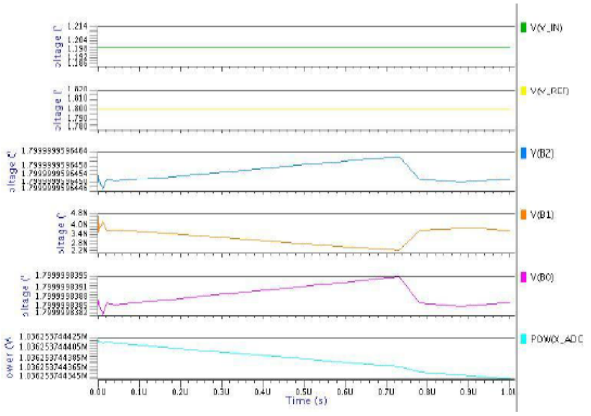

Fig.7: Simulated output waveforms of conventional CMOS based Flash ADC

In these waveforms, the values for Vin is set to be 2 and for Vref it is fixed at 3 and the reference voltage is given as Vref(i/2^n) for each comparator . When Vin is greater than Vref(i/2^n) the value obtained is 1 at the output of the respective comparator and in this case the output of the comparators come out to be 0011111. So as shown in the waveforms the digital word obtained at the output of encoder, i.e. V(B2), V(B1) and V(B0) is 101 respectively.

The simulation results of proposed architecture using transmission gate and GDI Technique are shown in figure 8(a) and 8(b) respectively.The input voltage Vin for these architectures is 2 and Vref is 3. The output of the comparator1is '1', which is same as bit B2 of the final output. And the output of the comparator2 is '0' which acts as a second bit of the final output. And the output of comparator3 is 1 which is B0 of the final ADC output. The final digital output obtained by using three comparators is 101.

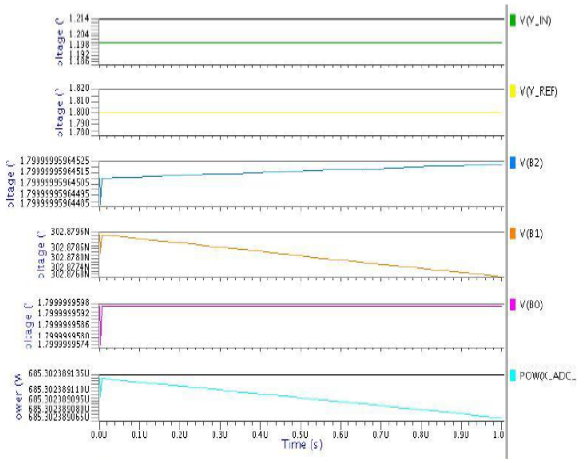

Fig.8(a): Proposed architecture using transmission gate

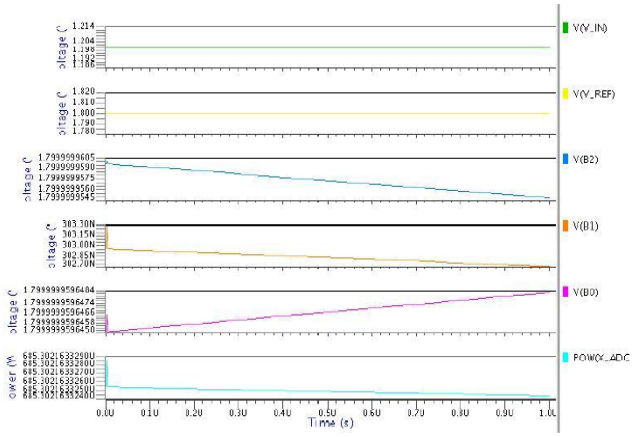

Fig.8(b): Proposed architecture using GDI Technique

Table 2. Performance comparison of all three types of 2x1 MUX designed using different technique

Technique Used	Power(pW)	Delay(ps)
CMOS	101.8	35.219
TG	56.8	31.693
GDI	8.41	27.234

From table 2 it is shown that the GDI technique dissipates power less than other techniques because the leakage power of GDI technique is less than others and has less transistor count in designing of same circuit. The propagation delay is also less in the GDI technique compared to others.

Table 3. Performance comparison of Flash ADC

Flash ADC	Transistor count	Power(µW)
Conventional Flash ADC	126	1036.25
Flash ADC using TG	54	685.30
Flash ADC using GDI	38	685.30

From table 3 it is clear that the power dissipated using conventional Flash ADC and transistor count is maximum and although the power dissipated for both proposed techniques is same but the transistor count is minimum for the GDI Technique.

5. CONCLUSION

In this paper, TG and GDI based power and area efficient 3-bit flash ADC is designed and implemented. In these configurations, the reference voltage is generated with less number of comparators and with the use of MUX. The MUX are designed using 3 different techniques and the one with GDI technique is the most efficient one with minimum power and delay. By using these configurations, first we can reduce the power; second, the transistor count is reduced. As compared to the conventional Flash ADC design, the proposed Flash ADC designs features best in power and transistor count.

6. REFERENCES

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