Abstract

SRAM is faster and more expensive and it is typically used for CPU cache. SRAMs are the fastest form of RAM available which does not need to be refreshed periodically. Here, 6T SRAM cell with O-ABB circuit is designed. On-chip adaptive body bias (O-ABB) circuit consists of standby leakage current (Iddq) sensor circuit, decision circuit and body bias control circuit which are used to compensate the effect of NBTI. Dynamic power is the power measured when circuit is in active mode. Here, Multi Threshold Complementary Metal Oxide Semiconductor (MTCMOS) technology is applied in the individual circuit of On-chip adaptive body bias to decrease the power. Low power MTCMOS methodology is applied in the proposed circuit which provides high performance and low power design. Design metrics such as Power, Delay and Power delay product are taken in to account. After applying MTCMOS technology, the power and the power delay product of the proposed circuit decreases when compared the existing circuit. All the circuits were designed using SYNOPSYS EDA tool and simulated in 28nm technology.
References


**Index Terms**

Computer Science

Circuits and Systems

**Keywords**

CMOS, MTCMOS, Power, Delay, Adaptive body bias.