Design of Low Power Barrel Shifter using Pulsed Latches

Surya A.

Department of electronics and Communication Engineering

Anjalai Ammal-Mahalingam Enginnering College

Kovilvenni, Thiruvarur

ABSTRACT

In this paper, a barrel shifter is a specialized digital electronic circuit with the purpose of shifting an entire data word by a specified number of bits by using combinational logic and sequential logic used. Multiplexer based 8-bit barrel shifter circuit is implemented using the hardware description language ―Verilog. The proposed barrel shifter architecture implementation shows reduction in power consumption

Keywords

Multiplexer, verilog HDL, power, pulsed latches, microwind.

1. INTRODUCTION

1.1 Barrel shifters

Barrel shifters are specialized electronic circuits used to shift the bits of binary data and often employed by embedded digital signal processors and other general-purpose processors in order to manipulate data. Data shifting is required for various low-level data applications such as floating-point arithmetic operations, bit indexing and variable-length coding. A barrel shifter is able to complete the shift in a single clock cycle, giving it a great advantage over a simple shifter which can shift n bits in n clock cycles. It is used in conjunction with a processor's arithmetic logic unit (ALU) or otherwise embedded in the ALU itself.[1]

A barrel shifter is able to shift the bits of binary data by moving it from one multiplexer to the next, with the supported number of bits dictated by how many multiplexers are used.

The formula for determining how many multiplexers are required is n log2(n)[where n is the number of bits supported. So for an 8-bit barrel shifter the calculation is $8 \times \log2(8) = 8 \times 3 = 24$

1.2 Pulsed latches:

Pulsed-latch circuits retain the advantages of both latches and flip-flops, offering higher performance and lower power consumption within a conventional ASIC design environment. Pulsed latch technique has been used to reduce the delay of various shift registers without increasing any power consumption.[3]

1.3 Multiplexer

The *multiplexer*, shortened to "MUX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple input lines called "channels" one at a time to the output [4].

2. OPERATING PRINCIPLE

2.1 Latches

When the clock is high, D flows through to Q as if the latch were just a buffer, but when the clock is low, the latch holds its present Q output even if D changes .Fig.1 shows the level triggered latch.[6]
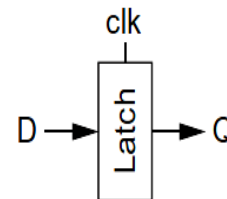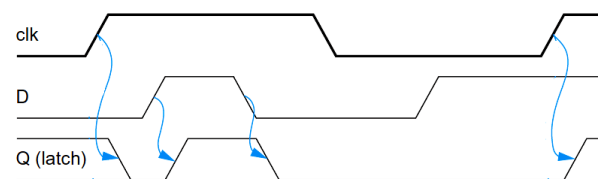

Fig.1 level triggered latch

Fig.2 timing diagram of latch

2.2 Pulsed Latch

Pulsed latch systems eliminate one of the latches from each cycle and apply a brief pulse to the remaining latch. [5]

If the pulse is shorter than the delay through the combinational logic, we can still expect that a token will only advance through one clock cycle on each pulse.
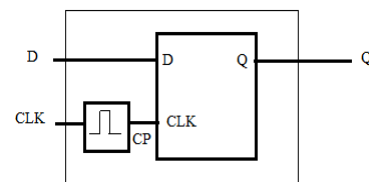
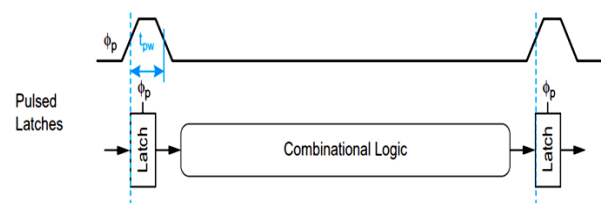In a pulsed system, the pulse width is tpw.

Fig.3 pulsed Latch

Fig.4 timing diagram of Pulsed latch

2.2.1 Max-Delay Constraints

The clock period must be at least,

Tc>max (tpcq + tpd, tpcq + tpd + tsetup- tpw).

Therefore, maximum allowable logic delay

tpd< Tc – max (tpcq, tpcq + tsetup- tpw)

2.2.2 Minimum Delay Constraint:

If the hold time is large and the contamination delay is small, data can incorrectly propagate throughtwo successive elements on one clock edge, corrupting the state of the system.

For Pulsed latch   : tcd>thold - tccq + tpw

2.3 Multiplexer

Digital multiplexer (MUX) selects binary information from one of many input lines and directs it to a single output line. Data selector (2 :1 MUX)[15]. Inputs: 2n data inputs, n select lines. Output: 1 data output line.The block diagram of 2-to-1 Mux is shown in figure.
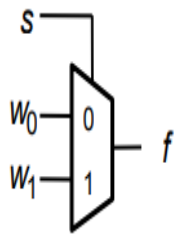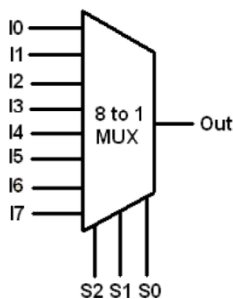

Fig. 5 Graphical symbol   Table.1 Truth table

2.4 Multiplexer

An 8-to-1 multiplexer is a digital device that selects one of the eight inputs lines to the output line by using three-bit selection line. The block diagram of 8-to-1 Mux is shown in figure.

S1	S2	S3	0
0	0	0	I1
0	0	1	I2
0	1	0	I3
0	1	1	I4
1	0	0	I5
1	0	1	I6
1	1	0	I7
1	1	1	I8

Fig. 6 Graphical symbol   Table.2 Truth table

2.5 Barrel shifter

A shifter is a combinational circuit with one or more inputs and an equal number of outputs. The outputs are shifted with respect to the inputs. If only a shift left or a shift right is required. A barrel shifter [4] is simply a bit-rotating shift register. The bits shifted out the MSB end of theregister are shifted back into the LSB end of the register. In a barrel shifter, the bits are shiftedthe desired number of bit positions in a single clock cycle. For example, an eight-bit barrelshifter could shift the data by three positions in a single clock cycle

Propagation delay is theoretically constant (at most one transmission gate), independent of shifter size, no. of shifts [12].

Shift and rotation units are useful in many different networks. Consider a 4-bit word a3a2a1a0 as the input into the general rotation unit shown in fig.

The output is a rotated word f3f2f1f0. A n-bit rotation is specified using the control word, while the L/R bit defines a left or right movement.

For example, a 1-bit left rotation yields an output of

f3f2f1f0 = a2a1a0a3

while a 1-bit right rotation gives

f3f2f1f0 = a0a3a2a1

3. CIRCUIT DIAGRAM

3.1 Conventional 8-bit Barrel Shifter using Multiplexer

The above circuit shows a multiplexer based 8-bit barrel-shifter[8]. The circuit allows rotating the input data word right, where the amount of rotating is selected by the control inputs. Several microprocessors include barrel-shifters as part of their ALUs to provide fast shift or rotate open.

The circuit shown above consists of three stages of 2:1 multiplexers. When all multiplexer select inputs are active (low), the input data passes straight through the cascade of the multiplexers and the output data (q7..q0) is equal to the input data (d7. d0). When S2control signal is selected, the first stage of multiplexers performs a rotate-right by one bit operation, due to their interconnection to the next lower input. Similarly, the second stage of multiplexers performs a rotate-right by two bits whenS1 control signal is selected. Here the corresponding multiplexer inputs are connected to their second next-lower input.

Finally, the third stage of multiplexers performs a rotate-right by four bits, when S0 control signal is selected.

Due to the cascade of three stages, all three rotate [9] operations (by one bit, by two bits, by four bits and so on) can be activated independently from each other. For example, when both S2 and S0 are activated, the shifter performs a rotate-right by five bits.[11]
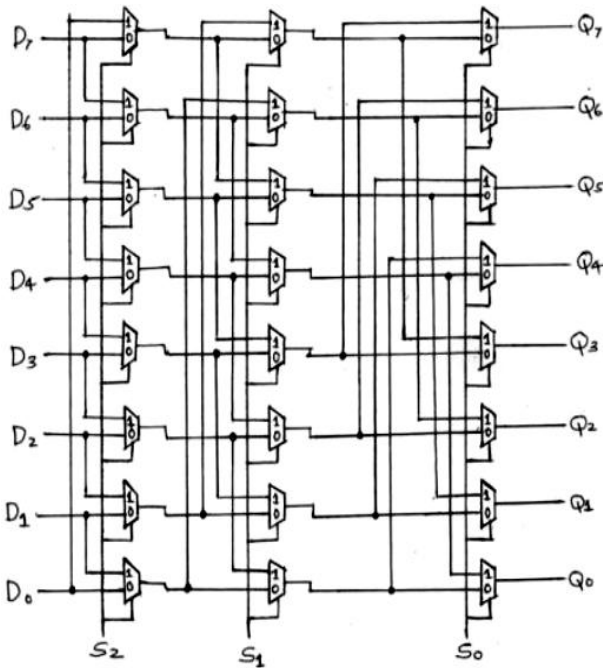
3.1.1 Port Specification

D7-D0	8-Bit Input
Q7-QO	8-Bit Output
S2-S0	3-Bit Select Lines
	If S0=1 ➔ Input Shift By 4 Bits
	If S1=1 ➔ Input Shift By 2 Bits
	If S2=1 ➔ Input Shift By 1 Bit

3.1.2 Rotate Operation:

The rotate operation is a shift where the bit which is shifted out of the vector LSB is inserted at its MSB.[10],[13]

3- Bit Opcode			Operation
Left	Rotate	Arithmetic	
0	0	0	Shift right logical
0	0	1	Shift right arithmetic
0	1	X	Rotate right
1	0	0	Shift left logical
1	0	1	Shift left arithmetic
1	1	X	Rotate left

3.1.3 Truth Table of Barrel Shifter

SELECT LINES			INPUT D[7:0]	OUTPUT D[7:0]
S0	S1	S2		
0	0	0	00001111	00001111
0	0	1	00001111	10000111
0	1	0	00001111	11000011
0	1	1	00001111	11100001

1	0	0	00001111	11110000
1	0	1	00001111	01111000
1	1	0	00001111	00111100
1	1	1	00001111	00011110

4. PROPOSED DESIGN:

4.1 8-Bit Barrel Shifter using 2:1 Mux and Pulsed Latches

In this arrangement [14], the latch is transparent only during a short time after the active clock edge, while it is opaque otherwise, regardless of the timing waveform of the clock. In other words, the latch behaves as an edge-triggered storage element. The pulsed latch cannot be used in shift registers due to the timing problem occurred in latch. This timing problem can be overcome with the use of multiple non-overlapped delayed pulsed clock signals. The delayed pulsed clocksignals are generated when a pulsed clock signal goes through delay circuits [16]
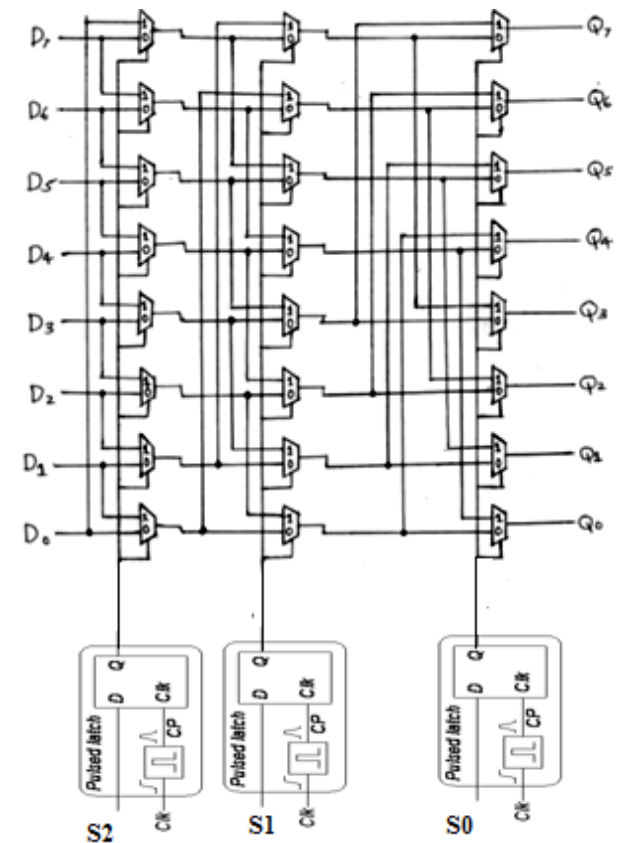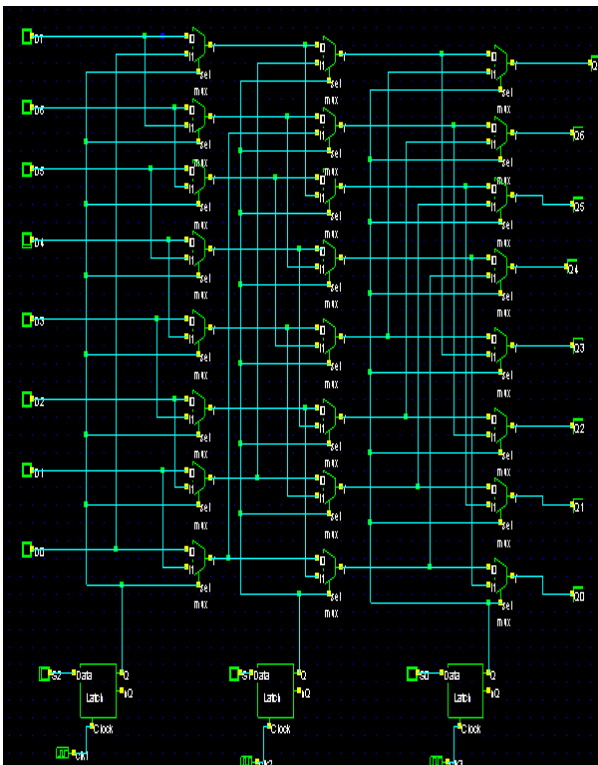

Table 3 .Power comparison

| Method	Power(μw)	Method	Power(μw)
Conventional (2:1 mux)	1.85	Conventional (8:1 mux)	0.35
Using pulsed latches	0.69	Using pulsed latches	0.32

5. SIMULATION RESULTS

Number of transistors connected to clock for pulsed latches [7] reduced to 12.5% and area is reduced to 57.6%.
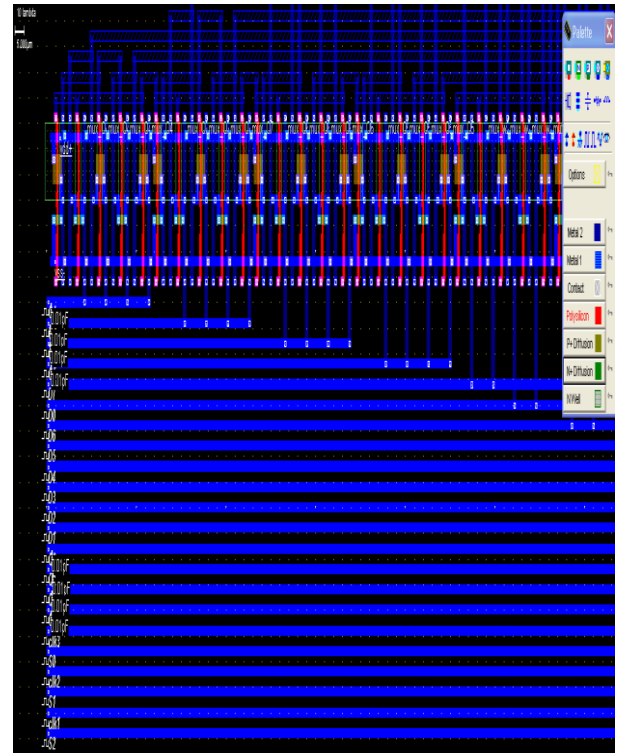
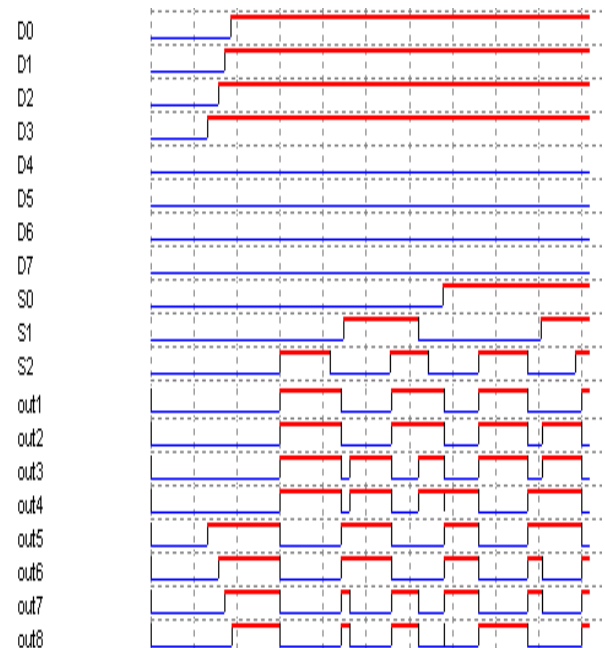The figure shows the barrel shifter using 2:1 mux and pulsed latch

The figure shows the barrel shifter using 8:1 mux and pulsed latch
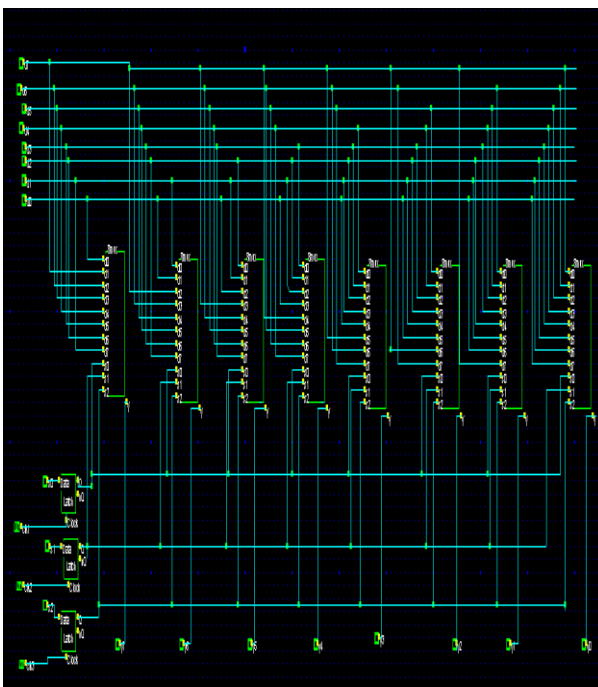
The figure shows the layout of the barrel shifter using mux and pulsed latches

The figure shows the timing diagram of the barrel shifter using mux and pulsed latches

6. REFERENCES

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