Integration and Performance Investigation of Multilevel Inverter with Half Bridge and Developed H-bridge Configurations

Mahwish Memon
Student of Master's in Electrical Engineering
Mehran University of Engineering and Technology Jamshoro

Mukhtiar Ahmed Mahar
Professor of Electrical Engineering
Mehran University of Engineering and Technology Jamshoro

Aneeqa Sattar
Student of Master's in Electrical Engineering
Mehran University of Engineering and Technology Jamshoro

ABSTRACT
This document introduces a new structure of power switches for Developed H-bridge with half bridge connected in cascade to provide increased of a nine-stepped output voltage inverter. The proposed model requires lesser number of switches and dc power sources, which results in decreasing the complexity of total cost of inverter. The multi-carrier pulse width modulation (LS-PD-PWM) method is designed to reduce the percentage of (THD) Total harmonic distortion. The output voltage THD is calculated using FFT analysis tool and is found to be 13.97%. The results taken by simulation are validated using MATLAB/SIMULINK software.

General Terms
Multilevel Inverter, Pulse Width Modulation (PWM), Semiconductor switches.

Keywords
Multilevel Inverter, POD-PWM, Cascaded H-Bridge inverter, MATLAB/Simulink Model.

1. INTRODUCTION
In nowadays electric power engineering investigator pay their interest on MLI to get high power quality, lower shift losses and reliable power for many industrial applications. [1] [2]. By using lesser number of DC sources as input with different structures of electronic switches these inverters generate staircase voltage waveform [3] a replacement topology has been planned with lesser number of DC voltage sources and lesser number of power switches. This paper proposes a simulation model for 9 level uneven cascaded Developed h-bridge with half bridge MLI arrangement The output voltage has been taken by utilizing phase opposition disposition arrangement (POD) technique. Review of different MLI topologies has been conducted. The output voltage waveform and THD analysis has been carried out.

The strategies of 3 standard MLI structures are available to generate levels output voltage waveform, i.e., neutral-point-clamped (NPCMLI) or diode clamped (DCMLI), flying capacitor (FCMLI) and cascaded H-bridge (CHBMLI) [4][5]. Multilevel inverters further cascaded arrangement is classified into two arrangements i-e asymmetric and Symmetric. [4][6].

In asymmetric arrangement DC sources are unequal in its H bridge, whereas in symmetric arrangement DC sources are equal. to output voltage waveform and reduce the THD and switching losses, different modulation methods are implemented. [7][8]

The specific arrangement of switches and modulation technique selection is dependent on the power requirement. Switching techniques are classified into two kinds of i.e., fundamental frequency switching and high frequency switching. [9][10] These techniques include selective harmonic elimination (SHE), phase shift, sinusoidal PWM and space vector [11] Mostly pulse width modulation (PWM) is widely used PWM. Also, divided into phase disposition arrangement (PD), phase opposition disposition arrangement (POD) and alternate phase opposition disposition arrangement (APOD) techniques [12][13].

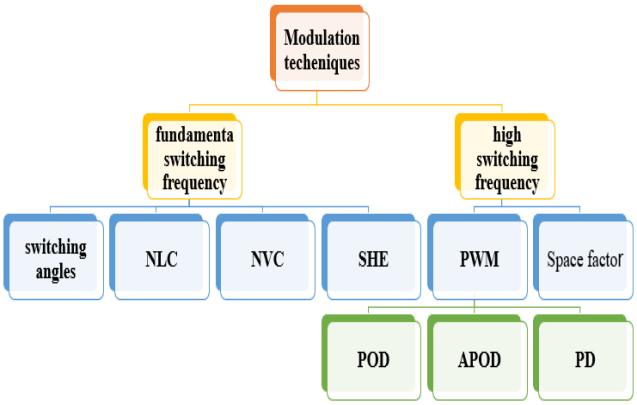

Fig 1: Classification of Modulation Techniques

2. METHODOLOGY
For the simulation of proposed model MATLAB/SIMULINK is the software used The THD of the output voltage wave is measured using FFT analysis tool in MATLAB/SIMULINK software.

Parameters for the Proposed simulation model taken are shown in table 1.

Table 1: Proposed Model Parameters

Frequency of Sine wave	50 Hz
Switching frequency of power switches	1000 Hz
Output voltage levels of Proposed Model	9
Resistive load	100Ω
Power Switches	IGBT
No. of switches used in Proposed Model	8
No. of DC voltages	3
Magnitude of DC voltages	V_1=V_2= 10 V V_3= 5 V

3. CASCADED CONNECTION OF DEVELOPED H-BRIDGE MLI WITH HALF-BRIDGE CONFIGURATION

3.1 BLOCK DIAGRAM OF PROPOSED TOPOLOGY

Figure 2 shows the block diagram of proposed model comprise of developed H-bridge MLI in cascaded fashion with half-bridge configuration

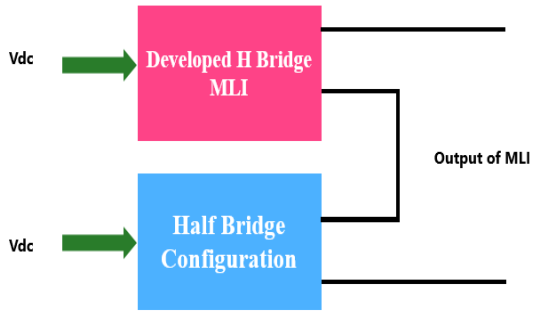

Fig 2: Block Diagram of proposed Model.

3.2 PROPOSED TOPOLOGY

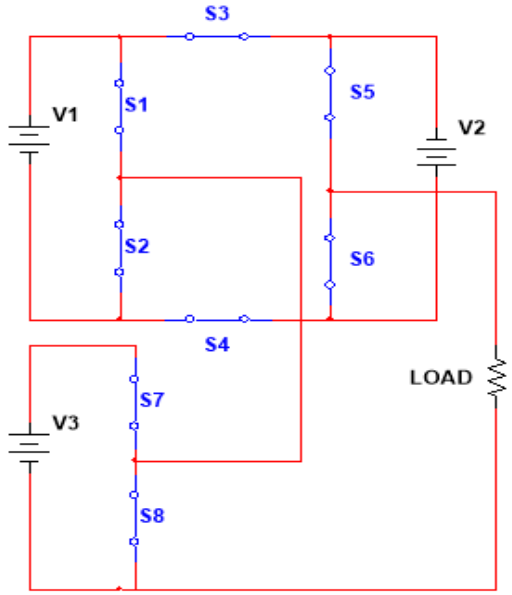

Fig. 3: Proposed Model for Nine-level inverter

Figure 3: shows A developed H-bridge electrical converter is extended by connected single phase half-bridge inverter with separate single Dc source. The main purpose of this series connected half-bridge inverter is to maximize the output voltage levels, reduce harmonic distortion (THD) and enhance power quality [7] [14].

The proposed topologies shown in figure 3 are comprising of by adding two more unidirectional switches and one voltage source DC to the developed H-bridge inverter structure i-e the proposed inverter topology is comprising of eight (8) unidirectional power switches that are (S1, S2, S3, S4, S5, S6, S7, & S8) and three voltage sources DC (V1, V2, & V3) in this paper the proposed model of inverter is called as cascaded connection of developed H-bridge and half bridge multilevel inverter (DHB-HB-MLI)

In figure 3 the simultaneously turn-on of (S1& S2) or (S5 & S6) or (S3 & S4) and (S7, & S8) causes voltage source as short circuited i-e to turn on simultaneously of these switches must be avoided.

If the DC sources V1 & V2 of developed h-bridge inverter are equal in magnitude i-e (2pu) with same polarity and voltage source V3 of Half bridge inverter with magnitude i-e (1pu) then levels of output voltage decrease to five.

If the DC sources V1 & V2 of developed h-bridge inverter are equal in magnitude i-e(2pu) with change in polarity and DC source V3 of Half bridge inverter with magnitude i-e (1pu) then levels of output voltage increase. i-e total output voltage levels will be nine-levels.

So, polarities of DC sources should be in asymmetric to create Maximum output voltage levels without increasing the quantity of switches. because by only changing the polarities of dc supply the output levels are increased by four levels also cost of proposed model will be less.

The DC sources magnitudes for proposed model of nine-level inverter shown in figure 3 are as follows

$$V1=2\ Vdc \quad (1)$$

$$V2=2\ Vdc \quad (2)$$

$$V3=Vdc \quad (3)$$

Considering eq (1,2, &3) for proposed nine level inverters, generates 0, ±Vdc, ± 2Vdc, ± (3Vdc), ±4Vdc at output.

4. SIMULATION MODEL

The proposed Model has been modelled in MMATLAB/ SIMULINK software, which is developed by MathWorks Inc. The POWERGUI tool has been used for THD and output voltage analysis.

4.1 MAIN CIRCUIT

This simulation model comprises of eight IGBT transistors It incorporates three DC sources of two 10V & one 5V. As seen in Fig 4.

The proposed model for asymmetric developed H-bridge with Half-bridge MLI comprises of eight IGBTs, and three dc voltage supply shown in Fig.4. To receive the 9-level stepped output, the switches are signaled using POD-PWM technique, according to the switching pattern of IGBT switches the respective operation modes for the proposed model described below.

In 1st mode, S2, S4, S6 & S7 switches are triggered to give output V3 (5V).

In 2nd mode, S2, S3, S5 & S8 switches are triggered to give output V1 (10V).

In 3rd mode switches S2, S3, S5 & S7 are triggered to give output V1+V3 (15V).

In 4th mode, switches S2, S3, S6 & S8 are triggered to give output V1+V2 (20V).

In 5th mode, switches S2, S3, S6 & S8 are triggered to give the output (0V).

In 6th mode, switches S1, S4, S6 & S7 are triggered to give output V3-V1 (-5V).

In 7th mode, switches S2, S3, S4 & S8 are triggered to give output -V2 (-10V).

In 8th mode, switches S1, S4, S5 & S7 are triggered to give output V2+V3-V1 (-15V).

In 9th mode, switches S1, S4, S5 & S8 are triggered to give output -V1-V3 (-20V).

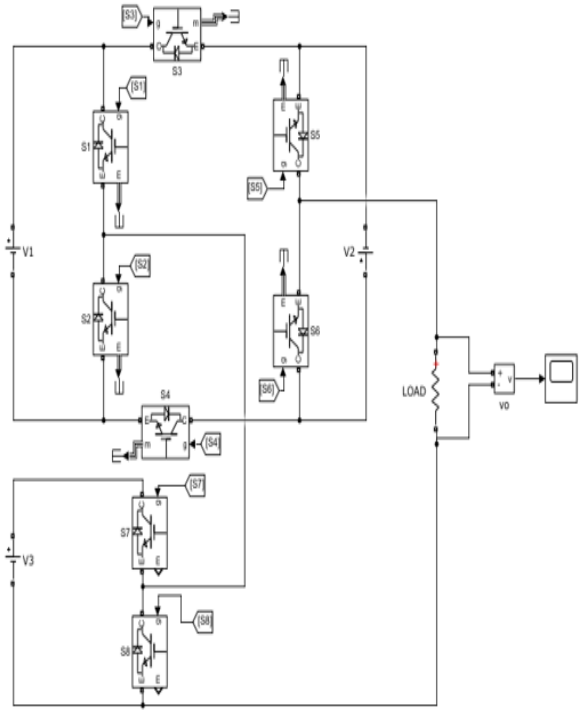

Fig. 4. Simulation Model for 9-level Asymmetric DHB with HB MLI

4.2 CONTROL CIRCUIT

The control circuit comprises of several comparators to generate the multicarrier waveform with POD technique. It can be seen in Fig. 5.

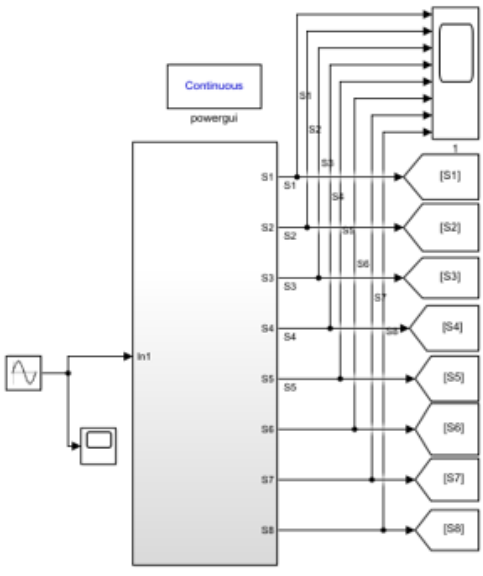

Fig 5: Control circuit of Proposed Model

Multi-carrier based PWM-POD is adopted to produce desired gating signals for power switches. The PWM-POD technique creates sufficient delay to trigger the switches accordingly to generate nine level voltage output waveforms

5. SIMULATION RESULTS

Based on proposed topology of cascaded developed h-bridge with half-bridge multilevel inverter (cascaded DHB-HB MLI) as shown in fig 4 has been used for simulation to verify performance of proposed DHB-HB-MLI in generating all output voltage levels (odd & even).

The proposed topology for cascaded DHB-HB MLI comprises of eight IGBT switches and three DC voltage sources shown in figure 4 to receive nine-level stepped output voltage waveform the switches are signaled by POD-PWM carries technique Each step has a difference of 5V as staircase shown in output waveform figure 6. This simulation is done by the usage of MATLAB/SIMULINK software

The total-harmonic-distortion is found to be 13.97%. THD waveform is shown in Figure 7.

The THD analysis was carried out working on FFT analysis tool of MATLAB/SIMULINK software.

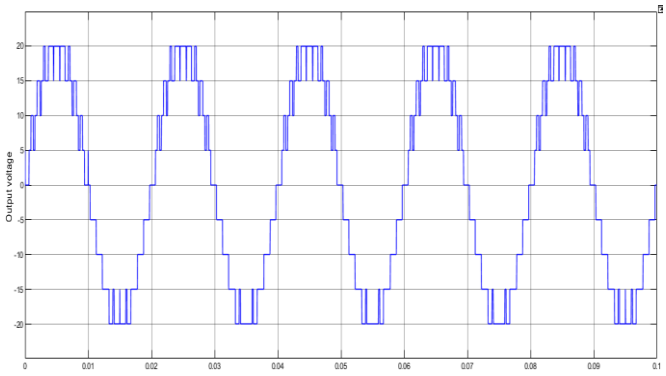

Fig 6: Output Waveform of Nine-level Voltage.

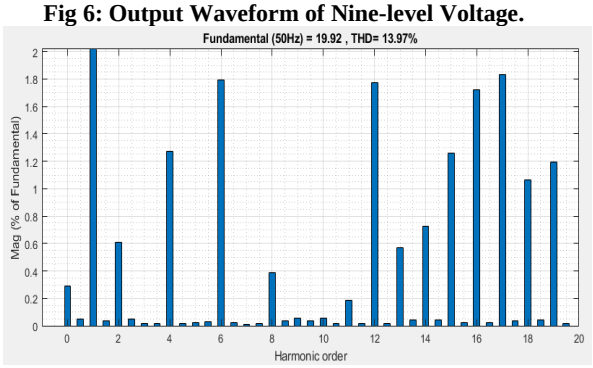

Fig 7: THD of Output Waveform of Nine-levels.

6. CONCLUSION

A simulation model of 9-level asymmetric cascaded Developed H-bridge with Half -bridge MLI has been modelled by eight power switches (IGBTs) with three sources of DC power. The FFT analysis of output voltage waveform is carried out at 19.92 and THD is found to be 13.97%. This Modified MLI can be interfacing with renewable energy sources such as PV cells and wind power It can be extended for motor drives, electric vehicle drives, power factor compensators and DC power source utilization. This Modified MLI chosen as the best option in the field of power industry, and reactive power compensation.

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