High Speed Compressor based Adder using XOR-XNOR Gate: A Study

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ABSTRACT
Multiplier is an essential block of a computing device. Multipliers are commonly used for signal and image processing applications where multipliers are used to perform various tasks like convolution, correlation and filtering. Multipliers are not only a high delay component but also dissipate high amount of power. It is necessary to increase the speed of multipliers as the demand of high speed processors is increasing. Moreover, multipliers is an integral part of any processor and are utilized by the processors to complete signal processing tasks. Optimizing performance of multipliers provides better results in digital signal processors. In multiplier, reduction of partial products takes more time and consumes high power. A huge number of adders are used to perform the partial product reduction operation. Optimizing the partial products reduction is a challenging task for researchers. Compressors take more inputs at a time and are able to process partial products in a faster way compared to conventional adders. Use of compressors in the partial product reduction helps to minimize the delay but not power consumption.

Keywords
Compressor, Compressor Based Adder, XOR-XNOR Gate, Different Input

1. INTRODUCTION
High speed, small area, low power and low cost are always expected by VLSI circuit engineers while designing for computing devices. Hand held devices such as mobile phones, laptops and phablets are becoming more and more popular everyday. Majority of the mobile users demand longer stand-by and talk time with higher operating frequencies. In CMOS, Deep Sub-Micron (beyond 65nm) transistors consume high static power. Practically, microprocessors or Digital Signal Processors (DSP's) have various complex signal processing modules such as audio and video compression, gaming and graphical modules to meet customer demands.

It leads the processors or ICs to be of higher density. It is necessary to minimize thepower dissipation in portable, higher density and Deep Sub-Micron (DSM) based devices. Low power design has several merits such as less cooling cost and improved reliability. Also, it reduces the weight and makes the devices compact. It is important to provide high performance portable devices and it may not be compromised for low power dissipation. Normally, signal processing applications perform several tasks such as convolution, filtering, FFT, DCT of the signal, masking, filtering, stretching and image multiplication tasks are performed in image and video processing applications [1, 2].

Multiplication can be performed in different ways. Hardware complexity of the serial multipliers is lower than parallel multipliers. Researchers have analyzed and proposed several new structures for parallel multipliers because parallel multipliers are faster in nature.

This is iterative and sequential multiplier. Repeated addition technique is used in this method. Multiplicand (M) bits are added with "N" times, where "N" is the size of multiplier. Fig. 1.1 shows the diagram of shift-and-add method. "N" bit multiplication is done with the help of Accumulator, ALU, registers for multiplicand and multiplier and control unit. The value of multiplicand is added and accumulated based on the LSBbit of multiplier. In every clock, multiplier bit is shifted right and the bit is tested. If the value is "1", multiplicand is added with accumulator and bits are shifted right else the accumulator value shifted right. This procedure repeats until all multiplier bits are tested. Finally, the result is in accumulator. The length of result is "2N" bits and this multiplier takes "N" cycle to complete the tasks. Conventional CISC machine uses this multiplier.

This multiplier belongs to parallel multiplier category. In this multiplier, all partial product are generated in parallel. time to compute the final result is smaller than serial multiplier. This multiplier is used in high performance systems. Array of addersare used in each rows and columns. As word length increases, it is possible to extend the multiplier structure without affecting the existing structure. Pipelining is possible inarray multiplier whereas sequential and tree multipliers do not support pipeline. Sinceit has regular structure, place, and route, interconnection of cells are simpler than other multipliers. Moreover, this multiplier provides the simple VLSI circuit layout.

2. LOGIC GATE
A logic gate is a position of controlled changes used to ascertain tasks utilizing Boolean rationale in advanced circuits. They are fundamentally completed electronically, however can similarly be built utilizing electromagnetic transfers, electronic diodes, liquids, optical or on the other hand even mechanical components. Cardinal attributes of the rationale entryways are:

- The ability to interface with single or two information wires
- The ability to interface with one yield wire
- The ability to get an incentive from an associated input wire
- The ability to convey an incentive to an associated yield wire
- The capacity to figure right yield esteem, given current info value(s).

The four kinds of fundamental rationale doors are AND, OR, XOR and NOT entryways. With these four, any possible Boolean condition can be gotten through. By the by, for accommodation, the determined kinds NAND, NOR and XNOR are additionally rehearsed, which frequently utilize less circuit components for a given condition than a usage based exclusively on AND, OR, XOR and NOT would do.

3. LITERATURE REVIEW

Tianqi Kong et al. [1], approximate multipliers are applicable in error resilient applications with relaxed precision constraints, including image processing, multimedia, and data recognition. Such multipliers that sacrifice some accuracy can gain a corresponding increase in electrical performance. This article presents ananalys is of the architectures of previously proposed compressors to investigate their performance and accuracy. In this article, we propose five high-accuracy approximate 4-2 compressors with better delay, area, power, and better performance–accuracy trade off. Pro1–Pro4 rely on the critical path optimization, whilePro5 derives from the modified sorting technique. This article implements 8 × 8 and 16 × 16 multipliers by employing the proposed approximate compressors in TSMC 28 nm. The experimental results indicate that our designs have about 18% delay,43%–52% area-delay product (ADP) reduction compared to the exact multiplier, and 20%–55% ADP optimization compared to compressors with the same accuracy. This article further verifies the efficacy of the proposed compressors through image blending and matrix multiplication applications.

A. G. M. Strollo et al. [2],approximate multipliers attract a large interest in the scientific literature that proposes several circuits built with approximate 4-2 compressors. Due to the large number of proposed solutions, the designer who wishes to use an approximate 4-2 compressor is faced with the problem of selecting the right topology. In this paper, we present a comprehensive survey and comparison of approximate 4-2 compressors previously proposed in literature. We present also a novel approximate compressor, so that a total of twelve different approximate 4-2 compressors are analyzed. The investigated circuits are employed to design 8 × 8 and 16 × 16 multipliers, implemented in 28nm CMOS technology. For each operand size we analyze two multiplier configurations, with different levels of approximations, both signed and unsigned. Our study highlights that there is no unique winning approximate compressor topology since the best solution depends on the required precision, on the signedness of the multiplier and on the considered error metric.

Z. Gu et al. [3], augmentation is a hypothetically more effective increase calculation than generally utilized Karatsuba and textbook duplication however is infrequently utilized in pragmatic equipment plans because of its inborn careful divisions, which are tedious and hard for equal and sequential speed increase. This brief proposes a technique for sans division Toom-Cook duplication based Montgomery secluded augmentation, which makes it workable for Toom-Cook increase to be applied in commonsense and effective equipment executions. We additionally give an equipment execution of measured multipliers of 256 pieces and 1024 pieces with benefits on region time-item over past explores.

R. Liu et al. [4], enormous whole number duplication is the basic activity to plan a secluded multiplier. Karatsuba algorithm (KO calculation) to divide the operands into two sections is for the most part used to plan a huge number multiplier. In this paper, we right off the bat propose a plan of 258-piece multiplier dependent on KO-3 calculation derived by KO calculation, with which equipment assets can be diminished than KO calculation. Then, at that point, we build a 256-cycle four-stage pipelined Montgomery secluded multiplier on the foundation of proposed multiplier. At last, we execute the plan of secluded multiplier on Virtex-6 FPGA stage. This plan can run at the clock pace of 68 MHz with 187.9k LUTs roughly. Furthermore, our plan can acquire the consequence of Montgomery secluded multiplier for each clock. Contrasted and different plans on FPGA, our plan shows a superior exhibition in term of region time item.

Ranjan Kumar Barik et al. [5], In this presents, a high-speed signed Vedic multiplier (SVM) architecture using redundant binary (RB) representation in Urdhva Tiryagbhyam (UT) sutra. This is the first ever effort towards extension of Vedic algorithms to the signed numbers. The proposed multiplier architecture solves the carry propagation issue in UT sutra, as carry free addition is possible in RB representation. The proposed design iscoded in VHDL and synthesized in Xilinx ISE 14.4 of various FPGA devices. The proposed SVM architecture has better speed performances as compared with various state-of-the-art conventional as well as Vedic architectures.

Basant Kumar Mohanty et al. [6], transpose form finite-impulse response (FIR)filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike direct-form configuration. In this paper, explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter. Its have derived a general multiplier-based architecture for the proposed transpose form block filter for reconfigurable applications. A low-complexity design using the MCM scheme is also presented for the block implementation of fixed FIR filters. The proposed structure involves significantly less area- delay product (ADP) and less energy per sample (EPS) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure.

L kholee phim et al. [7], parallel FIR channel is for the most part utilized among different sorts of channel in Digital Signal Processing (DSP). This paper demonstrates the structure of zone proficient 2-parallel FIR channel utilizing VHDL and its execution on FPGA utilizing picture framework. This paper gives the subtleties fundamental squares of region productive 2-parallel FIR advanced channel. In this paper proposed 2-parallel advanced FIR channel and territory effective 2-parallel FIR channel are clarified. Its reproduction utilizing Xilinx 14.2 are likewise talked about. It likewise introduces the FPGA execution of essential 2-parallel channel and zone productive 2-parallel on Xilinx 14.2 Spartan 3E Starter Board XC3S500E chips and its outcomes. Since adders are light weight in silicon territory when contrast and the multipliers, along these lines multipliers are supplanted by the snake to lessen zone and postponement of the parallel FIR channel. Xilinx ISE is utilized for mimicking the structure of the channel.

Vijaya Lakshmi Bandi et al. [8], productive design is the present major worry in the field of VLSI, Digital flag handling circuits, cryptographic calculations, remote correspondences and Internet of Things (IOT). Greater part of the designs utilizes increase. Acknowledgment of duplication by utilizing dreary expansion and move what's more, include techniques expends more territory, power and postponement. Vedic is one of the effective multipliers. Plan of Vedic multiplier utilizing unique sutras decreases zone and power. From the structure of Vedic multiplier, it is obviously watched that there is degree to plan a productive engineering. In

this exploration, Vedic multiplier is outlined utilizing changed full snake which devours less number of LUT's, cuts and postpone when contrasted with ordinary customary Vedic multiplier.

G. Challa Ram et al. [9], describes the design of high speed Vedic multiplier that uses the techniques of Vedic mathematics based on 16 sutras (algorithms) to improve the performance. The efficiency of Urdhva Tiryagbhyam (vertical and crosswise) Vedic method for multiplication which is different from the process of normal multiplication is presented. Urdhva -Tiryagbhyam is the most efficient algorithm that gives minimum delay for multiplication for all types of numbers irrespective of their size. Vedic multiplier is coded in Verilog HDL and stimulated and synthesized by using XILINX software 12.2 on Spartan 3E kit. Further the design of array multiplier is compared with the proposed multiplier in terms of delay, memory and power consumption.

S. P. Pohokar et al. [10],briefly describes the Urdhva- Tiryagbhyam Sutra of Vedic mathematics and we have designed multiplier based on the sutra. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras which are discovered by Sri Bharti Krishna Tirthaji. In this era of digitalization, it is required to increase the speed of the digital circuits while reducing the on chip area and memory consumption. In various applications of digital signal processing, multiplication is one of the key components. Vedic technique eliminates the unwanted multiplication steps thus reducing the propagation delay in processor and hence reducing the hardware complexity in terms of area and memory requirement. We implement the basic building block: 16×16 Vedic multiplier based on Urdhva-Tiryagbhyam Sutra. This Vedic multiplier is coded in VHDL and synthesized and simulated by using Xilinx ISE 10.1. Further the design of array multiplier in VHDL is compared with proposed multiplier in terms of speed and memory.

4. EXCLUSIVE OR LOGIC GATES

The Exclusive OR logic gate is one of the logic gates that perform an exclusive or operation; i.e, a true output results if one, and only one, of the inputs to the gate is true. A false output results if both the inputs are false and both are true. XOR represents the inequality function, i.e., the output is high if the inputs are unalike otherwise the output is low. A way to think XOR is 'one or the other, but not both'. XOR can also be seen as addition modulo-2 and it can also called as arithmetic gate. Because of this, XOR gates are utilized to perform binary addition in computers. A basic digital adder is the half adder, which adds two bits, that comprises of an XOR gate for sum and an AND gate for carry. The algebraic expressions A.B1 +A1 .B and (A+B).(A 1 +B 1) either used to represent the XOR gate with inputs A and B and the operation of exclusive OR is summarized in the below truth table named as Table 1.1. XNOR is complementary to XOR. Applications of Exclusive OR logic gates are: The Exclusive OR circuit is the basic building block of various circuits mainly arithmetic circuits like adders, multipliers, compressors, comparators, pseudo random number generators, parity generators or checkers, code converters, correlation &sequence detectors, error detecting and error correcting codes, phase detector circuit in PLL and encryption processor. Hence it is used widely in many VLSI systems as a section of the critical path that determines the altogether performance of the system. So enhancing the performance of the XOR gate is important in reducing the propagation delay and power consumption.

Table 1: Two input Exclusive OR Truth Table

A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

5. METHODOLOGY

A compressor adder is a logical circuit which is used to improve the computational speed of the addition of 4 or more bits at a time. Compressors can efficiently replace the combination of several half adders and full adders, thereby enabling high speed performance of the processor which in corporates the same. The compressors used in the proposed architecture are explained as-

4:2 Compressor

A 4:2 compressor is capable of adding 4 bits and one carry, in turn producing a 3 bit output. The 4-2 compressor has 4 inputs X_1, X_2, X_3 and X_4 and 2 outputs Sum and Carry along with a Carry-in (C_{in}) and a Carry-out (C_{out}) as shown in figure 3.1. The input C_{in} is the output from the previous lower significant compressor.

The C_{out} is the output to the compressor in the next significant stage. The critical path is smaller in comparison with an equivalent circuit to add 5 bits using full adders and half adders.

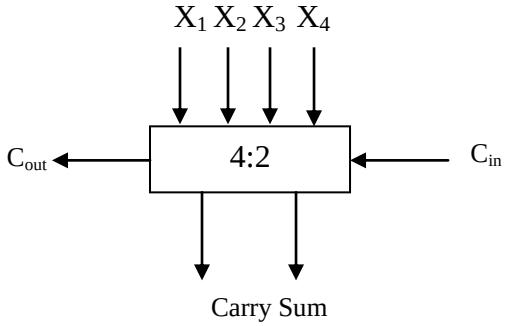


Fig. 1: Block Diagram of 4:2 Compressors

Similar to the 3-2 compressor the 4-2 compressor is governed by the basic equation

$$X_1 + X_2 + X_3 + X_4 + C_{in} = sum + 2*(Carry + C_{out}) \quad (1)$$

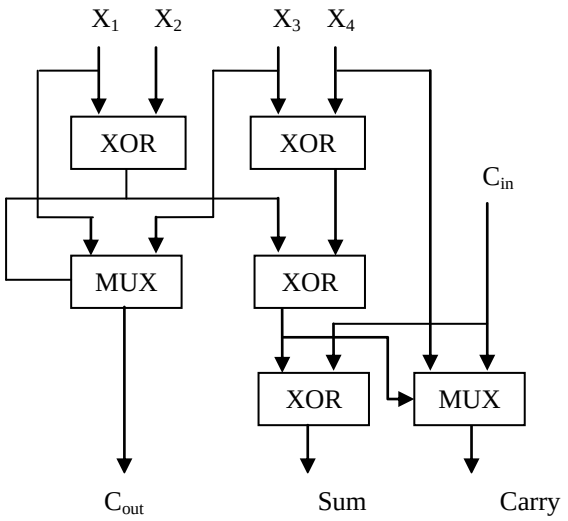
The standard implementation of the 4-2 compressor is done using 2 Full Adder cells as shown in figure 2.When the individual full Adders are broken into their constituent XOR blocks, it can be observed that the overall delay is equal to 4*XOR.

Modified 4:2 Compressor

The block diagram in figure 3 shows the existing architecture for the implementation of the 4-2 compressor with a delay of 3*XOR. The equations governing the outputs in the existing architecture are shown below

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{in}$$

$$C_{out} = (X_1 \oplus X_2).X_3 + (X_1 \oplus X_2).X_1$$



$$C_{arry} = (X_1 \oplus X_2 \oplus X_3 \oplus X_4).C_{in} + (\overline{X_1 \oplus X_2 \oplus X_3 \oplus X_4}).X_4$$

Fig. 3: Logical Diagram of Modified 4:2 Compressor

In show the delay and area all the modified 4:2 compressors. 4:2 compressors replacing some XOR blocks with multiplexer's results in a significant improvement in delay. Also the MUX block at the SUM output gets the select before the input arrive and thus the transistors are already switched by the time they arrive.

6. CONCLUSION

Various two input and three input XOR and XNOR cells are reviewed from the past to the most recent published research work. (ii) Eight circuits of two new structures for two input XOR/XNOR circuits and compared with existing circuits with respect to parameters like propagation delay, power consumption and noise margin. (iii) Three circuits for three input differential XOR/XNOR circuits and compared with existing circuits with respect to all parameters. (iv) Four input differential XOR/XNOR circuit and compared with existing circuits with respect to all parameters. (v) General structure for multi input XOR/XNOR circuits, where that structure can be used for minimum of fan-in four to any number.

7. REFERENCES

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