# Design and Performance Assessment of Asymmetric Structure of Developed H-bridge Multilevel Inverter Configurated with Double-Level Circuit

Saiqa Channa
Student of Master's in Electrical Power Engineering
Mehran University of Engineering and Technology Jamshoro

Mukhtiar Ahmed Mahar
Professor at the Department of Electrical Engineering
Mehran University of Engineering and Technology Jamshoro

Abdul Sattar Larik
Professor at the Department of Electrical Engineering
Mehran University of Engineering and Technology Jamshoro

## ABSTRACT
A single-stage thirteen-level MLI is suggested in this paper based on the developed Hybrid bridge MLI configured with the double-level circuit. Though the concept of a double-level circuit was already introduced it is still not utilized. This topology will not only lessen the number of devices but also increase the output of an inverter twice that of the conventional cascaded hybrid bridge multilevel inverter. The purpose of this network topology is to enhance the output of the Multilevel inverter reduce the component count of devices used and utilize the concept of double level circuit. A pulse width modulation with a Phase disposition technique is used with the asymmetric structure of three DC sources V1=12, V2=24, and V3=48 to obtain a greater number of levels. The design of this suggested topology is done by using MATLAB software. An analysis is also carried out using the FFT tool in MATLAB software.

## Keywords
Developed H-bridge, Asymmetric, Double level circuit, Reduced device count.

## 1. INTRODUCTION
In the field of power electronics, multilevel inverters have gained the focus of in-depth research. The topologies, different control strategies, modulation techniques, and utilization of MLIs have always been the subject of various research investigations and academic publications[1]. Numerous multilevel inverters with different topologies have been proposed, including the flying capacitor, CHB inverter, and diode-clamped (neutral-point clamped) inverter[2]. There are benefits and trade-offs associated with complexity, cost, and performance for each topology. Control schemes are essential for the operation of multilevel inverters. Different control strategies, such as carrier-based PWM, SVM, and SHE, have been studied by researchers[3]. These techniques aim to develop ideal switching patterns that lower the total harmonic distortion and enhance quality and efficiency[4][7]. Researchers have concentrated on modulation techniques for multilevel inverters. To produce the required output voltage waveform with low harmonic distortion and high-quality performance, several strategies have been suggested[10], including hybrid modulation methods, sinusoidal PWM, and harmonic injection PWM. Multilevel inverters have huge numbers of applications They have been successfully integrated with wind turbines and solar photovoltaic systems[15], among other renewable energy systems, where they improve grid integration and optimize power extraction[5]. To obtain high power density and run the motor more smoothly, multilevel inverters are also used in electric vehicles. Moreover, they are essential to grid-connected systems, grid-tied energy storage, and high-power industrial drives[16].

Out of all the topologies, the cascaded hybrid bridge has gained more attention than other topologies because of its numerous advantages[9]. Researchers have done remarkably well to develop topologies of cascaded hybrid bridge-based MLIs to improve the quality of multilevel inverters[15]. The concept of double-level circuits has been introduced but is still not well utilized[6]. In this research, a control strategy is suggested that fully utilizes the concept of a double-level circuit[11]. A 13-level inverter is proposed based on a developed hybrid asymmetric bridge configured with the double-level circuit. In contrast to the previous topologies[13][10], it doubles the output of MLI making the output waveform more sinusoidal with less harmonic distortion. Moreover, the proposed topology uses a smaller number of devices. The suggested network configuration is designed using MATLAB Software. A PWM technique is used to produce a staircase waveform.

## 2. METHODOLOGY
The suggested topology in this research is simulated using MATLAB/SIMULINK software as can be seen in Figure 2. The network topology uses three DC sources with asymmetric configuration. The output voltage waveform is analyzed using the Fast Fourier tool in MATLAB.

**Table 1. Parameters of the proposed topology**

| | |
|---|---|
| Frequency of reference signal | 50 HZ |
| Switching of power IGBTs | 1000 HZ |
| Output waveform levels | 13 LEVEL |
| Resistive load | 100 OHM |
| No of IGBT's | 6 |
| No DC sources | 3 |
| Magnitude of DC sources | V1= 10V V2=20V V3=5V |

## 3. SCHEMATIC DIAGRAM OF SUGGESTED MLI
The Schematic diagram of the suggested topology can be seen in Figure 1.

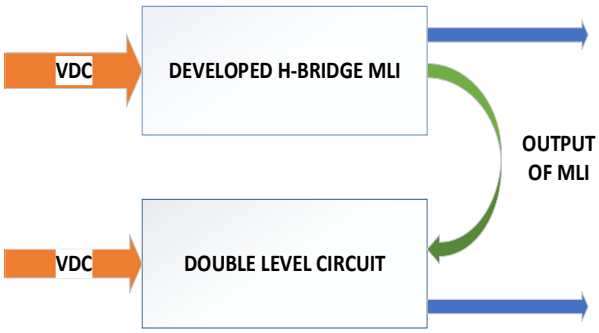



**Fig 1. Schematic diagram of suggested MLI network**

## 3.1 PROPOSED TOPOLOGY

Figure 3 shows the suggested topology for single phase 13 level MLI at resistive load. The topology suggested in this paper is comprised of a full hybrid bridge inverter with a half-bridge circuit[14]. The half-bridge will act as a double-level circuit in this topology. Though the concept of double level circuit has been already introduced but was not utilized. In this topology, the double-level circuit is used. The purpose of using DLC is to increase the output and voltage levels and to reduce harmonics and waveform distortion[8]. To obtain a greater number of levels, the asymmetric configuration of DC voltage sources is used[17]. The voltage of DLC is half the voltage of a full bridge[12]. The magnitude of asymmetric three DC sources used for the suggested network topology is calculated as,

$$V_1 = 1Vdc \quad (1)$$

$$V_2 = 2Vdc \quad (2)$$

$$V_3 = 1/2Vdc \quad (3)$$

In this proposed multilevel inverter topology, the count of switches, gate trigger circuits, and DC voltage sources can be calculated as follows.

$$Ns = Ngd = 2n+6 \quad (4)$$

$$Ndc = 2n+1$$

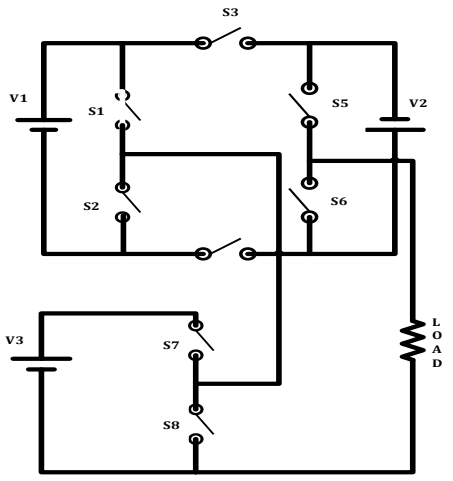



**Fig 2. Proposed topology**

## 3.2 MODULATION TECHNIQUE

The proposed topology is modulated using multicarrier PWM with a phase disposition technique. A sinusoidal waveform is considered a reference signal. Twelve carrier waves are required for the generation of 13-level output. The phase disposition technique is used because of its ability to modulate the wave with less harmonic distortion and distortion factor.

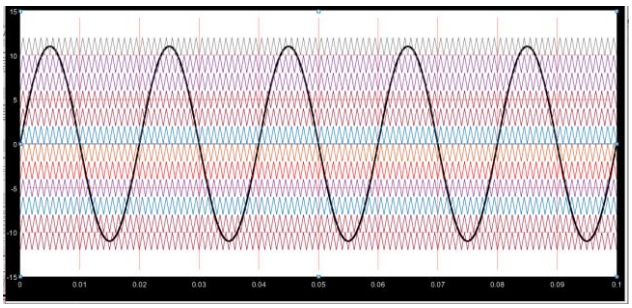


**Fig 3. PD Technique**

## 3.3 MODELING AND ANALYSIS

The suggested topology is designed using MATLAB SIMULINK. Eight IGBT switches are used being antiparallel to each other with three DC sources. A resistive load is used to observe the output of 13-level Developed H – H-Bridge MLI.

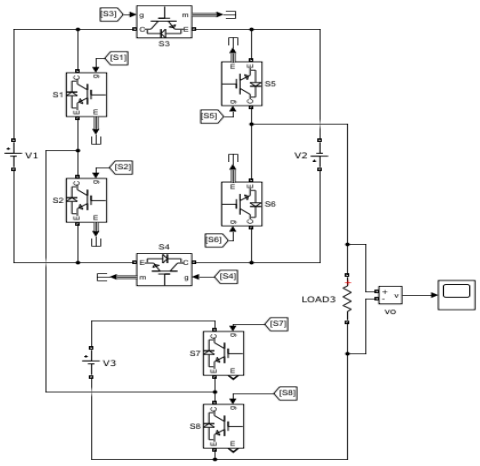



**Fig 4. Simulation model of Suggested topology**

## 3.4 CONTROL CIRCUIT

The control circuit of the suggested MLI configuration can be seen in Figure 5. The control circuit contains various logical operators and comparators to generate 13-level output voltage with the PD technique

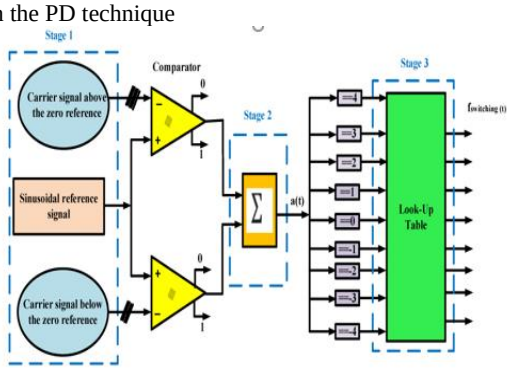



**Fig 5. The control circuit of the 13-level inverter**

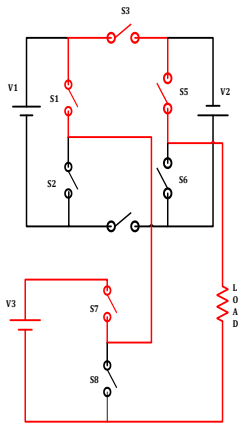
**Table 2. Switching table for the proposed topology**

| LEVELS | OUTPUT VOLTAGE | COMBINATIONS | SWITCHING |
|---|---|---|---|
| 1 | 5V | V3 | S1, S7, S3, S5 |
| 2 | 10V | V1 | S2, S3, S4, S8 |
| 3 | 15V | V1+V3 | S2, S3, S5, S7 |
| 4 | 20V | V2 | S6, S8, S1, S3 |
| 5 | 25V | V2+V3 | S6, S7, S1, S3 |
| 6 | 30V | V1+V2 | S6, S8, S2, S3 |
| 0 | 0V | 0V | S1, S3, S5, S8 |
| -1 | -5V | -V1+V3 | S1, S4, S5, S7 |
| -2 | -10V | -V1 | S1, S7, S6, S4 |
| -3 | -15V | -V2+V3 | S4, S2, S7, S5 |
| -4 | -20V | -V2 | S4, S2, S8, S5 |
| -5 | -25V | -V1-V2+V3 | S4, S1, S7, S5 |
| -6 | -30V | -V1-V2 | S1, S4, S8, S8 |

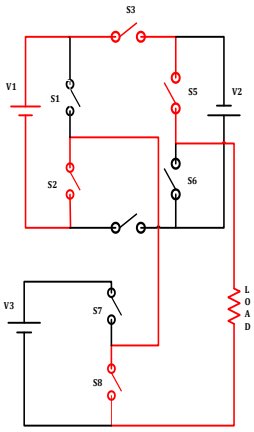
## 3.5 OPERATING MODES

Following are the modes of operation of the suggested topology. To obtain the thirteen-level output the proposed MLI circuit is made to operate in 12 different modes. The twelve modes are divided into positive and negative output levels

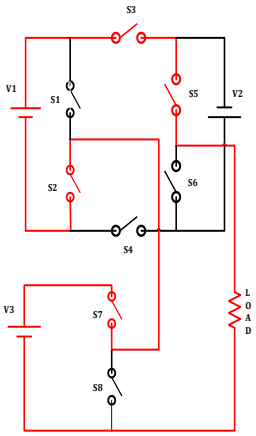
MODE 1



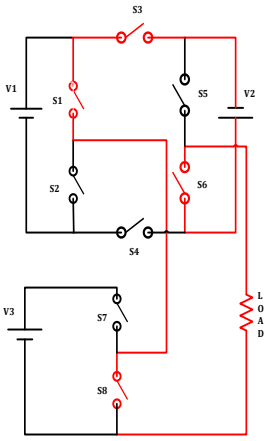

MODE 2



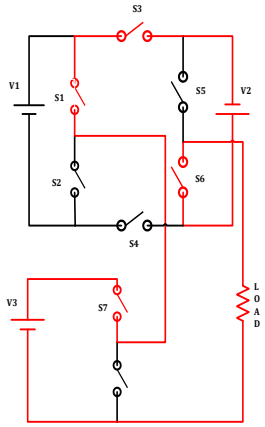

MODE 3



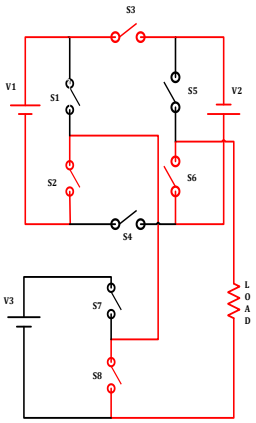

MODE 4



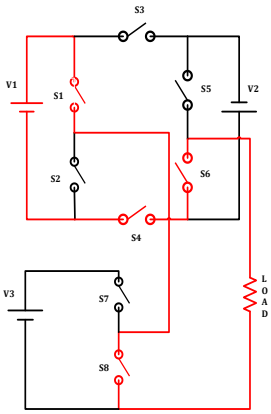

MODE 5



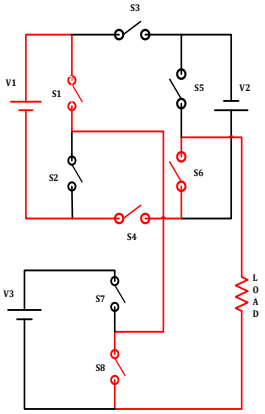

MODE 6

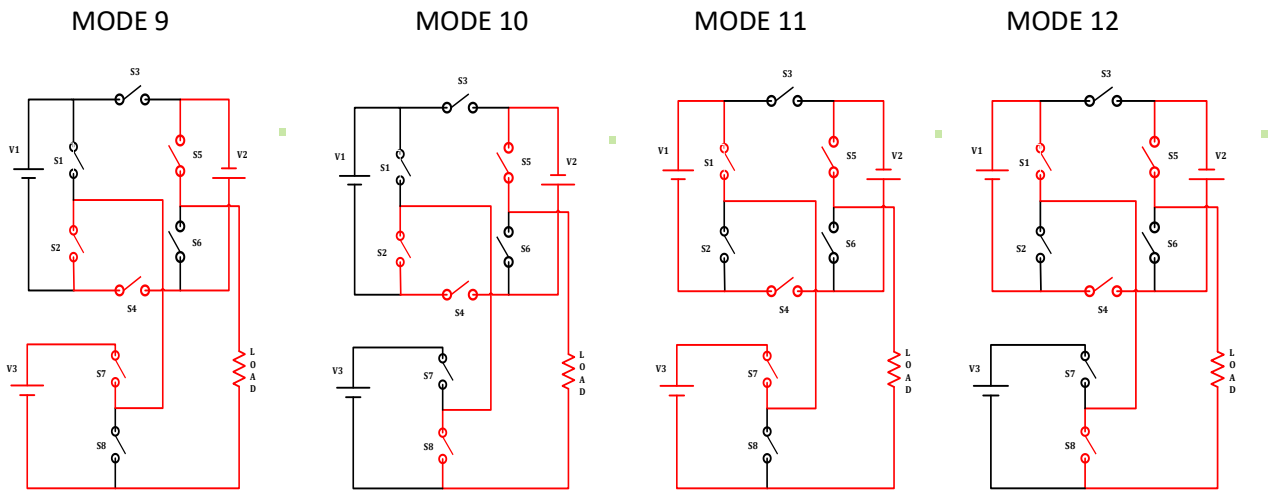



MODE 7




MODE 8






## 3.6 SWITCHING PATTERN

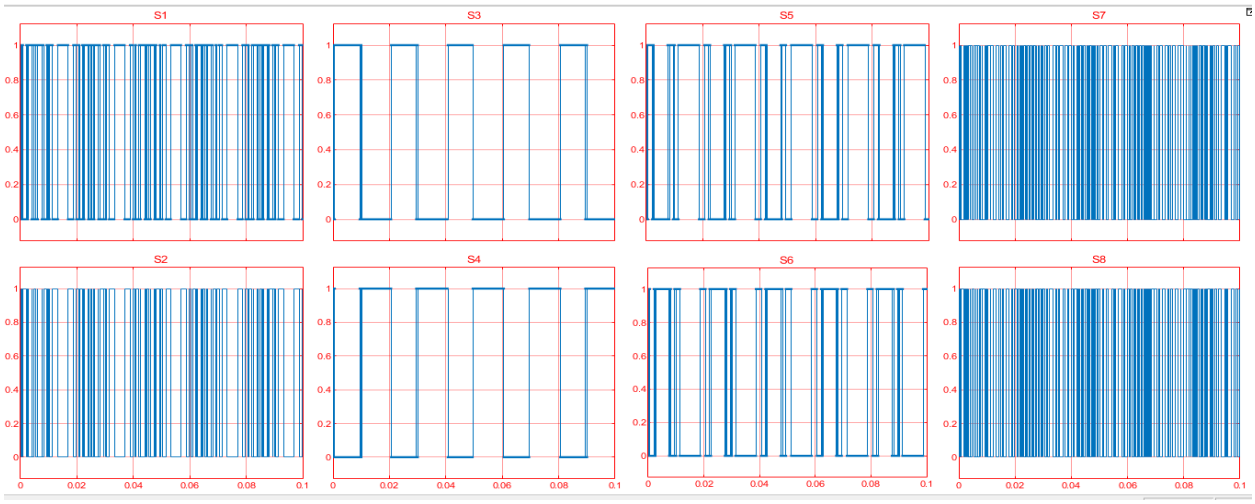



**Fig 6. Switching pattern of IGBTs with PD-PWM Technique**

**Table 3. Comparison of Proposed topology with other Existing topologies**

| TOPOLOGY | LITERATURE | NO OF SWITCHES | NO OF DC SOURCES | NO OF LEVELS | ThD |
|---|---|---|---|---|---|
| **Symmetric RDC MLI with DLC circuit** | Proposed in [6] | 8 | 3 | 9 | 13.97 |
| **Single Phase MLI with DLC circuit** | Proposed in [5] | 14 | 4 | 13 | 9.6 |
| **CHB With DLC** | Proposed in [11] | 14 | 4 | 5 | -- |
| **Developed CHB RDC MLI** | Proposed in [14] | 10 | 3 | 7 | 6.9 |
| **Asymmetric Developed CHB with DLC** | The proposed topology in this paper | 8 | 3 | 13 | 10.72 |

## 4 RESULTS

The suggested network topology is designed in MATLAB /SIMULINK. Figure 7. shows the output of the 13-level inverter.

Eight IGBTs with a switching frequency of 10000 HZ are signaled by using the PD technique.

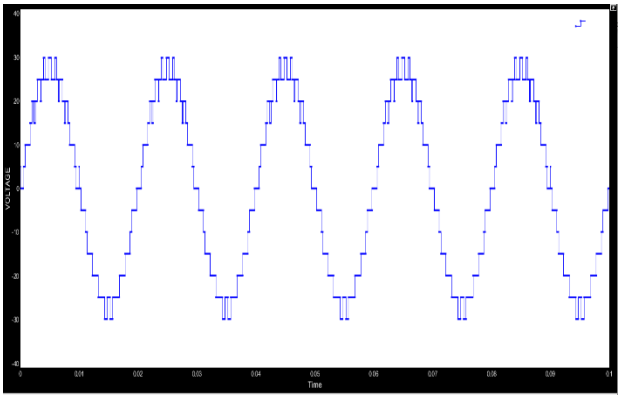


**Fig 7. The staircase output waveform of 13 -level Inverter**

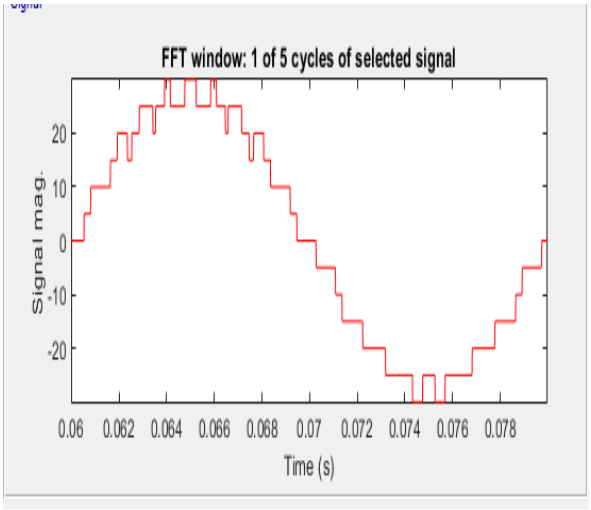



**Fig 8. FFT Analysis**

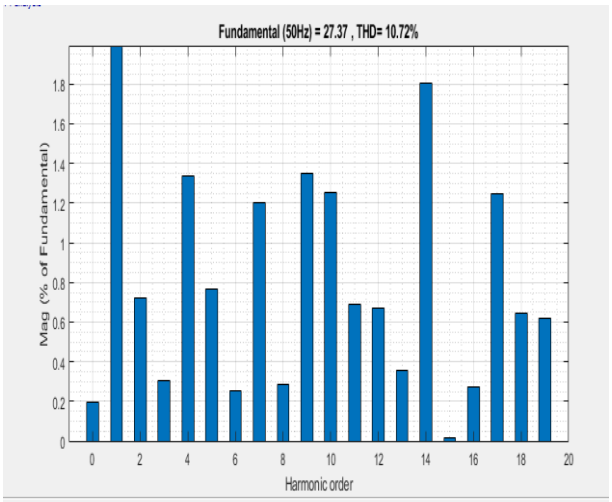



**Fig 9. Total harmonic Distortion of Proposed 13 level inverter**

## 5 CONCLUSION

In this report, research is conducted for the double-level circuit of multilevel inverters, and a topology is proposed. A thirteen-level inverter is proposed in this research based on the developed H Bridge configuration. The topology significantly reduces the number of components count and produces thirteen-level output with less harmonic distortion and variation. The purpose of developing this model was to utilize the concept of double-level circuits and to get a greater number of levels by using less number of devices. The whole model is developed using a software called MATLAB, and the output of the multilevel inverter can be seen in Figure 7. The total harmonic distortion is also carried out by using FFT TOOL in MATLAB. In contrast to other topologies, the suggested topology has less THD. Moreover, the present work can be extended in the future by integrating it with renewable energy sources like solar, wind, and biomass.

## 6 ACKNOWLEDGMENTS

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