This paper proposes buffer cache architecture. The proposed model consists of three units – main buffer cache unit, pre-fetch unit and LRU Evict Unit. An algorithm is proposed to retain the
evicted entry from main buffer cache unit in the LRU Evict Unit thereby giving it a second chance of access. On subsequent access in the LRU Evict Unit, the entry is promoted to the pre-fetch unit to accommodate more entries in the main buffer cache unit. On access in the pre-fetch unit, an entry is fetched into the main buffer cache. The LRU replacement policy is used in all the units. The proposed model is compared with buffer cache architecture with LRU replacement algorithm. The performance is comparable for sequential input where as 3% improvement in performance is seen for random input.

**Reference**

- Jong Min Kim, Jongmoo Choi, Jesung Kim, Sam H. Noh, Sang Lyul Min, Yookun Cho, Chong Sang Kim, A Low-Overhead High-Performance Unified Buffer Management Scheme that Exploits Sequential and Looping References, OSDI, 2000
- Mukesh Kumar Chaudhary, Manoj Kumar, Mayank Rai, A Modified Algorithm for Buffer Cache Management, IJCA, No. 12, Article 8
- Song Jiang and Xiaodong Zhang, LIRS: An Efficient Low Inter-reference Recency Set Replacement Policy to Improve Buffer Cache Performance, Proc. of SIGMETRICS 2002
- Theodore Johnson, Dennis Shasha, 2Q: A Low Overhead High Performance Buffer Management Replacement Algorithm, Proceedings of the Twentieth International Conference on Very Large Databases, 1994

**Index Terms**

Computer Science  
Database Systems
**Key words**

Buffer cache architecture          Least Recently used
Performance of database management system