This paper proposes buffer cache architecture. The proposed model consists of three units – main buffer cache unit, pre-fetch unit and LRU Evict Unit. An algorithm is proposed to retain the
evicted entry from main buffer cache unit in the LRU Evict Unit thereby giving it a second chance of access. On subsequent access in the LRU Evict Unit, the entry is promoted to the pre-fetch unit to accommodate more entries in the main buffer cache unit. On access in the pre-fetch unit, an entry is fetched into the main buffer cache. The LRU replacement policy is used in all the units. The proposed model is compared with buffer cache architecture with LRU replacement algorithm. The performance is comparable for sequential input where as 3% improvement in performance is seen for random input.

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Index Terms

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Buffer cache architecture            Least Recently used
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