Abstract

The main aim of this paper is to design and implement a high speed, low complexity and polymorphic architecture for reconfigurable folded wavelet filters. 5/3 wavelet results are incorporated into the 9/7 data path which reduces the number of adders compared to other solutions and also allows on the fly switching between the filters. The proposed work is to improve the speed of this reconfigurable architecture. This is accomplished by scheduling. A weight based scheduling algorithm has been used in this paper. This is an analysis method to improve inter task communication as well as data dependencies among tasks which will reduce the overall communication overhead and processing time.

Reference

- A. Pande and J. Zambreno, “Design and analysis of efficient reconfigurable wavelet
filters,” in IEEE International Conference on Electro/ Information Technology

Index Terms

Computer Science

System Architecture

Key words

Wavelet Architecture

DWT

Polymorphism