Abstract

The paper presents the implementation of MAC (multiplier-accumulator) unit using Vedic multiplier. The speed of MAC depends on the speed of the multiplier. The Vedic multiplier uses “Urdhva Tiryagbhyam” algorithm. The proposed MAC unit is coded in VHDL, synthesized and simulated using Xilinx ISE 10.1 software. The MAC is implemented on a FPGA device.
XC2S200-6PQ208 using Xilinx ISE10.1 tool. The proposed design shows improvement of speed over the design presented in [1].

Reference


Index Terms

Computer Science

Algorithms

Key words

MAC Vedic multiplier VHDL Carry Save Adder