Abstract

Field programmable gate arrays (FPGAs) are becoming increasingly important implementation platforms for digital circuits. This paper focuses on the implementation of Adaptive Infinite Impulse response (IIR) filter on an FPGA using Modified Particle Swarm Optimization (PSO) Algorithm. The proposed Filter is capable of finding the global optimum solution for system
identification problem in less number of iterations. The modified PSO algorithm has been developed and simulated using MATLAB. The result shows the enhanced speed of purposed design in terms of number of iterations it takes to identify the unknown system. The same algorithm has also been realized on various Xilinx FPGA devices and performances have also been analyzed. The area utilization by the proposed design on different FPGA devices has been compared. The results show that proposed filter is consuming very less area in terms of LUTs and Slices to provide enhanced area efficiency.

Reference

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**Index Terms**

Computer Science  
Signal Processing

**Key words**

FPGA  
IIR Filter  
LUTS  
MATLAB  
PSO