Abstract

As process technology shrinks, the adaptive leakage power compensation scheme will become more important in realizing high-performance and low-power applications. In order to minimize total active power consumption in digital circuits, one must take into account sub-threshold leakage currents that grow exponentially as technology scales. This describes to
predict how dynamic power and sub-threshold power must be balanced. The exclusive supply voltage control switching makes stable operations. The threshold voltage control successfully maintains a ratio of switching to leakage current and which represents the reduced power consumption. The goal of this paper is to: i) Maintains the optimized body bias conditions. ii) Maintains the best power-delay tradeoff. The results with a 180-nm CMOS device explain that the proposed architecture causes in the successful optimization of power.

Reference


Index Terms
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**Key words**

- CMOS
- leakage current
- supply voltage control
- threshold voltage
- control
- switching current