Abstract

Accumulate Repeat Accumulate -Low Density Parity Check Codes (ARA-LDPC) are a class of linear block codes having self error correcting capabilities. It is used to transmit messages efficiently over noisy transmission channels. Due to this, the probability of information loss can be made as small as possible. The inherent feature of these codes is that the data transmission rate approaches Shannon limit, which is the theoretical maximum data transfer rate for a
particular noise level. The ARA codes have a fast encoder structure and a protograph representation which allows for high speed iterative decoding. Because of these unique features, the ARA-LDPC codes are the most suitable for deep space applications. In this project, an architectural model of ARA-LDPC encoder is designed and simulated in Modelsim, synthesized using Xilinx ISE, for sequential, pipelined and wave pipelined architectures and the performance is analyzed in SYNOPSYS and XILINX environments. The most efficient wave pipelined architecture is implemented in Spartan 3E FPGA for a block size of 1024 bits.

Reference


Index Terms

Computer Science

Data Communications
Key words

ARA-LDPC decoder architectures
wave-pipelining