Abstract

The most research on the power consumption of circuits has been concentrated on the switching power and the power dissipated by the leakage current has been relatively minor area. In today’s IC design, one of the key challenges is the increase in power dissipation of the circuit which in turn shortens the service time of battery-powered electronics, reduces the long-term reliability of circuits due to temperature-induced accelerated device and interconnects
aging processes, and increases the cooling and packaging costs of these circuits. In this paper the main aim is to reduce power dissipation. A new design method for various logical circuits design, which is low power, compared to general Static CMOS logic. In this technique both NMOS transistor and PMOS transistors in various logic circuits is split into two transistors. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor Leakage current flowing through the PMOS transistor stack reduces due to the increase in the source to substrate voltage in the top PMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor. The tool used is TANNER EDA for schematic simulation. The simulation technology used is MOSIS 180nm.

Reference

- “Low Power CMOS Inverter design at different Technologies” International journal of applied engineering research, Dindigul Volume 1, No 3, 201010. “Low Power CMOS Inverter design at different Technologies” International journal of applied engineering research, Dindigul Volume 1, No 3, 2010

**Index Terms**

Computer Science

Circuits

**Key words**

Stack 6T SRAM cell low power

threshold voltage