Abstract

Gate-leakage reduction is the key motivation for the replacement of SiO2 with alternative gate dielectrics. 45nm gate length scaled grooved and bulk nMOSFETs are evaluated to bring out the most compatible and power saving dielectric option using Si3N4 and SiO2 using Silvaco ATLAS device simulator. At the scaled thickness, SiO2 controls the leakage better than Si3N4,
Enhanced Leakage Control in Scaled 45nm nMOS Devices using SiO2 and Si3N4

whereas at increased thickness of the dielectric Si3N4 proves better for the field scaled grooved and bulk devices with enhanced subthreshold slopes of 51.3mv/dec and 70mv/dec respectively. The field scaled device grooved at single sharp corner may be used for HP applications whereas field scaled bulk device may be used for LP and LSTP applications. This work can be helpful to device engineers working towards achieving ultra low power applications.

Reference

- Brice Tavel, 2004 “Gate dielectric impact for the 65nm Digital and Mixed Signal Platform Applications” Philips Semiconductors, Crolles2Alliance, Crolles, France

Index Terms

Computer Science

Integrated Systems
Key words

Grooved MOSFET        bulk MOSFET        dielectric
leakage power

scaled device

dissipation