Compact CPLD Board Designing and Implemented for Digital Clock

Abstract

The work describes the design and implementation of Complex Programmable Logic Devices (CPLDs) board for many digital applications in the educational and research field laboratory in the university. The objective of designed board is to implement the digital logic, which can be used for any digital application and take advantages of CPLDs features like reconfigurable architecture, high speed operation, pin locking, in-system programming (ISP) for digital system design. This CPLD board size is relatively compact; so it can be easily mounted. On board power supply and variable frequency oscillator improves functionality of overall board. The design includes some cost effective embedded control and communication interface to build digital application to work more efficiently in the market.

Reference

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Index Terms
Electronics CPLD Design

Key words
Reconfigurable architecture
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Digital Design
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