Abstract

Network on a chip can be viewed as processors with various instruction sets residing on a chip. Programs issued to a particular processor type can be divided into sequential and parallel code. Each subtask is characterized by an estimated time for completion. This paper proposes a method to determine the topological arrangement of processors to minimize the total execution time. The tasks are assumed to be allocated based on the algorithm proposed in literature. The logical arrangement of processors is in a directed acyclic connected graph. This is achieved in a tree arrangement. The expression for total execution time in this topology is derived. The model is simulated and the model verified.

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