Abstract

The fast Hartley transform and algorithm for DHT was introduced by Bracewell. The split radix decimation-in-frequency algorithm that requires less number of operation counts as compared to the radix-2 and radix-4 algorithms was developed by Sorenson et al. In this paper, an analog architecture for a split radix decimation-in-time algorithm is proposed. It utilizes three different
structures in the signal flow diagram. It exhibits a recursive pattern and is modular. The validity of the analog architecture is tested by simulating it with the help of the Orcad PSpice.

Reference


- AD-844 data sheet, Monolithic operational amplifier, Analog Devices, Rev-C.


Index Terms

Computer Science
Signal Processing

Key words
Decimation-in-time
Radix-2
Radix-4
Split-Radix

An Analog Architecture for Split-Radix DHT