Abstract

The demand for high speed, low power and low cost for Viterbi decoding especially in wireless communication are always required. Thus this paper presents the design of an adaptive Viterbi decoder that uses survivor path with parameters for wireless communication in an attempt to reduce the power and cost and at the same time increase the speed. Viterbi Algorithm is the
optimum-decoding algorithm for convolutional codes and has often been served as a standard technique in digital communication systems for maximum likelihood sequence estimation. The Add-Compare-Select (ACS) and Trace Back (TB) units and its sub circuits of the decoder have been operated in deep pipelined manner to achieve high transmission rate. In this paper register exchange based survivor unit is used as they have better throughput when compared to trace back using memory. Branch metric is calculated for either upper or lower half of trellis, which leads to reduction of power consumption. The Trellis code structure is divided into two segments. The first segment of the Trellis works in normal Viterbi mode while the second works in modified T-algorithm. The designed Adaptive Viterbi Decoder is able to detect and correct up to four errors. The design is optimized with respect to time, area and power and the netlist is generated. The netlist obtained after synthesis undergoes the physical design process. The synthesized circuits are placed and routed in the standard cell design environment and implemented on a Xilinx FPGA device.

Reference

- Rex Andrew Antony, “An Adaptive threshold strategy for soft decision Viterbi Decoder”, Dalhouse University, December 2002

Index Terms

Computer Science Wireless Communication
Key words
Convolutional Encoder
Adaptive Viterbi Decoder
Survivor Path
FPGA Implementation