Adders are one of the widely used digital components in digital integrated circuit design. The Carry Select Adder (CSA) provides a good compromise between cost and performance in carry propagation adder design. However, conventional CSA is still area-consuming due to the dual ripple carry adder (RCA) structure. In this paper, modification is done at gate-level to reduce
area and power consumption. The Modified Carry Select-Adder (MCSA) is designed for 8-bit, 16-bit, 32-bit and 64-bit and then compared with conventional CSA respective architectures. MCSA shows reduction in area and power consumption in comparison with conventional CSA with small increase in delay.

Reference

- Akhilesh Tyagi, “A Reduced Area Scheme for Carry-Select Adders”, IEEE International Conference on Computer design, pp.255-258, Sept 1990

Index Terms
Computer Science  Integrated Circuits

Key words
- Multiplexer
- Performance
- Adder
- VLSI and data paths