Abstract

Decimation filter is used to reduce the sampling rate for succeeding stages of an oversampling ADC. The speed of a successive-approximation ADC predominately depends on the decimator speed. This necessitates a need to design a high speed decimation filter to improve the overall system performance. A reconfigurable architecture is applied for the design
of decimator to serve this purpose. Results show that delay of a Reconfigurable Decimator is reduced by 29.74% compared to a Normal Decimation filter. The Number of Slices and 4 Input LUTs are reduced by 6% and 7% each, which reduces the Area.

Reference

- Clive Maxfield "The design warrior's guide to FPGAs: devices, tools and flows".

Index Terms

Computer Science
Signal Processing

Key words
oversampling
successive
approximation ADC
reconfigurable architecture