Abstract

At-speed testing has emerged as dominant test requirement in the era of high speed microprocessors. Since the conventional testing techniques prove to be incompetent, Instruction-Based Self-Testing (IBST) has been proposed as an effective alternate to those conventional techniques for at-speed testing of high performance microprocessors. The
Superscalar architectures, with vast functionality and exceptionally high speed have become the central integral part of modern high speed digital systems. However, testing superscalar microprocessors using this approach faces serious challenges, due to the out-of-order execution with multiple functional units and in-order commit behaviour. This paper discusses the test program generation procedure (template based) for multiple identical functional units in a superscalar architecture. Procedures for delay fault testing, which make sure that generated test vectors are applied in the correct order to test each testable path, are developed. The preliminary work has been presented in EWDTS[1]

Reference

Technique for Template Generation for Simultaneous Testing of Multiple Identical Functional Units in Super-scalar Architecture

- M. Hatzimihail et al., A Methodology for Detecting performance Faults in Microprocessor Speculative Execution Units via Hardware Performance Monitoring”, in Proc. of International Test Conference
- G. Theodorou et al., “A Software Based Self-Test Methodology for In-System Testing of Processor Cache tag Arrays”, in Proc. of International On-Line Testing Symposium (IOLTS) 2010

Index Terms

Computer Science
Electronic Testing

Key words
Superscalar Architecture And Test Challenges
Pipeline Vs Superscalar Processors
Technique for Template Generation for Simultaneous Testing of Multiple Identical Functional Units in Superecalar Architecture