Abstract

With ever increasing power density and temperature variations within high density VLSI chips, it is very important to study the temperature effects on the devices in a compact way and to predict their scaling. In this paper, the sub-threshold leakage power analysis of the P3 and P4
SRAM cells has been carried out at a temperature range from -250C to +1250C. It has been observed that the sub-threshold leakage and the standby power dissipation increases with increase in temperature. However, due to the stacked pMOS design used in P4 and P3 SRAM cells, minimum sub-threshold leakage and standby leakage power is observed as compared to the conventional 6T design.

References


Index Terms

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Analysis of the Effect of Temperature Variations on Sub-threshold Leakage Current in P3 and P4 SRAM Cells at Deep Sub-Micron CMOS Technology

**Keywords**

- Temperature Effect
- Sub-threshold Leakage
- Standby Leakage Power
- Conventional 6T SRAM Bit-cell
- PP-SRAM
- P4-SRAM
- P3-SRAM
- Stacking
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