Aerospace applications contain accelerometers that are realized with FIR filter using DA (distributed arithmetic) algorithm. When the DA algorithm is directly applied in FPGA to realize
FIR filter, it is difficult to achieve the best configuration in the coefficient of FIR filter i.e. the storage resource and the computing speed. To overcome the above difficulty we proposed an improved DA algorithm. This algorithm uses splitted LUTS which results usage of small memory and operational speed increases. The specifications of decimation FIR filter will be derived from the specifications of a third-order single bit sigma-delta modulator. We propose higher order decimation FIR filter i.e. 48th order implementing with less hard ware complexity. The hardware model for the filter was realized using verilog HDL.

References

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**Index Terms**

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