A Novel Approach to Reduce Leakage Power in GALS System architectures

Abstract

Globally asynchronous locally synchronous (GALS) system architectures are known for low power consumption through clock gating techniques. In GALS architectures set of logical
synchronous modules will communicate with other through asynchronous wrappers. Though this technique results in good dynamic power consumption, as the process technology shrinking down to 45nm and below the leakage power is equivalent to dynamic power consumption. In this paper, we are proposing a power gating technique for GALS architectures which uses existing handshaking signals of asynchronous wrappers to reduce both dynamic and leakage power consumption. To prove the proposed architecture we have implemented a GALS asynchronous micro controller from Daltons[1] synchronous 8051. For this we used Synopsys SAED 90nm library for synthesis and demonstrated the new proposed power gating control techniques through U.P.F (Unified Power Format) based simulation results.

References


Index Terms

Computer Science  Integrated Circuits
Keywords

GALS (Globally asynchronous locally synchronous)

Power Gating

Power Gating Control

U.P.F (Unified Power Format)

Clock Gating

4-Phase Hand Shaking