In this paper an efficient approach is presented to design and implement Direct Digital Frequency Synthesizer (DDFS) with high speed and spectral purity for wireless applications like Software Defined Radio (SDR). The implementation is based upon efficient utilization of embedded slices and LUT’s of the target device to enhance the speed of the proposed design. The proposed DDFS is designed & simulated with MATLAB and Xilinx AccelDSP, synthesized with Xilinx Synthesis Tool (XST) and implemented on Spartan 3E & Virtex 2P based XC3S500E and XC2VP307FF896 FPGA target device respectively. The proposed design can operate at an estimated frequency of 116.2 MHz and 146.5 MHz, along with the minimum period of 8.605 ns and 6.8240 ns for the Spartan 3e and Virtex 2 Pro FPGA device, respectively. The FFT analysis of developed DDFS shows enhanced SFDR of 86.17dB.

References

Efficient FPGA Implementation of Direct Digital Frequency Synthesizer for Software Radios


Index Terms

Computer Science

Communication Systems
Keywords
DDFS; FFT; FPGA; SDR and SFDR.