Abstract

The paper orients to develop a strategy, with a view to ensure that the output voltage is equally shared among a number of Single Ended Primary Inductance Converters (SEPICs), in addition to ensuring regulation of the load voltage. It attempts to exploit the robustness of a Variable Structure Controller (VSC) to offset the circuit parasitic and extract a stable output irrespective of the variations in input voltage, circuit parameters and/or load. The methodology envisages characterizing the desired time response and acclaiming an acceptable steady state and transient results. It involves the use of a Field Programmable Gate Array (FPGA) to implement the proposed scheme and illustrate its practical viability. The performance evaluated through MATLAB based simulation is adequately validated using a suitable prototype to project its applicability over a preferred operating range.

References

FPGA Implementation of Voltage Sharing Strategy for Series Connected SEPICS

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