Abstract

A glitch compensation methodology is proposed in this paper which involves in reducing the undesired switching of combinational circuits in order to save dynamic power. The proposed methodology can be seamlessly integrated to existing physical design flow to reduce the glitch power which is one of the major contributing factors for both dynamic and IR drop. A glitch is an undesired transition that occurs before intended value in digital circuits. A glitch occurs in CMOS circuits when differential delay at the inputs of a gate is greater than inertial delay, which results into notable amount of power consumption. The glitch power is becoming more prominent in lower technology nodes. Introduction of buffers at the input of the Logic gate may reduce glitches, but it results into large area overhead and dynamic power. Hence, the proposed methodology will ensure low dynamic power consumption with less area. The pass transistor logic is used as a compensation circuit and a flow is also proposed for characterizing the pass transistor logic to cater different delay values. The proposed methodology has been validated using Synopsys 90nm SAED PDK.
A Technique to Reduce Glitch Power during Physical Design Stage for Low Power and Less IR Drop

References


Index Terms

Computer Science

Integrated Circuits

Keywords

Dynamic power  digital logic circuits  low power design  CMOS delay devices  simulation

glitches