VLSI Architecture of Digital Auditory Filter for Speech Processor of Cochlear Implant

Abstract

Digital VLSI implementation of an auditory filter for speech processor of cochlear implant (CI) is proposed. Optimized design for hardware implementation of the filter with respect to area, power and speed is the significant criterion for the implementation of auditory filter for a CI. A digital filter is designed using the System Generator 10 through the mathematical model of the FIR filter developed in Simulink using FDA tool. It is further downloaded onto the Spartan 3E FPGA Kit. Translation of the Simulink model into a hardware realization is done using system generator. Thus simulation is done both in the hardware and software environment. VHDL code for the filter is developed using the coefficients generated from FDA tool of System generator. The area, power and delay analysis for the design is done using SYNOPSYS Design Vision tool with 180micron technology.

References

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Index Terms

Computer Science       Signal Processing

Keywords

Keywords—Cochlear implant (CI) Finite-impulse response filter (FIR) area power speed