Abstract

Parallel processing can be used to design high performance computing systems. In a parallel computer inter-connecting processors and linking them efficiently to the memory modules is not an easy task. Therefore, there is a requirement of an interconnection network that provides the desired connectivity and performance at minimum cost. Multistage interconnection networks (MINs) provide cost-effective, high-bandwidth communication between processors and/or memory modules in comparison to bus and crossbar interconnection networks. In this paper a new irregular MIN named IFTN (Improved Four Tree Network) has been proposed. The performance of IFTN has been measured in terms of reliability and cost. It has been proved that the proposed network IFTN provides much better fault-tolerance and reliability at lesser cost In Comparison To Four Trees.
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**Index Terms**

Computer Science

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