Abstract

In this paper we present control flow prediction (CFP) in parallel register sharing architecture to achieve high degree of ILP. The main idea behind this concept is to use a step beyond the prediction of common branch and permitting the architecture to have the information about the CFG (Control Flow Graph) components of the program to have better branch decision for ILP. The navigation bandwidth of prediction mechanism depends upon the degree of ILP. It can be increased by increasing control flow prediction at compile time. By this the size of initiation is increased that allows the overlapped execution of multiple independent flow of control. The multiple branch instruction can also be allowed. These are intermediate steps to be taken in order to increase the size of dynamic window to achieve a high degree of instruction level parallelism exploitation.

Reference
- Vijay S. Pai, Parthasarathy Ranganathan, Hazim Abdel-Shafi, Sarita Adve, “The Impact of Exploiting Instruction-Level Parallelism on Shared-Memory Multiprocessors”, IEEE

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Index Terms

Computer Science

Computer Architecture

Key words

CFP

ISB

ILP

CFG

Basic Block