Abstract

The exponential increase in test cost is one of the new challenges being posed by technology scaling. This Paper has been aimed to deal with the issue of testing cost which adds to the chip cost. Here we propose a new pattern set for testing the arithmetic circuits which contains a minimum number of test vectors and easy to generate on the chip and hence supports at-speed testing of the circuit. Though maximum fault coverage is desired but practically generation of test vectors for testing of all the possible defects is not at all feasible. This leads to the modeling of defects as faults which facilitate for simplification of test generation process. Though various fault models have been proposed, the single stuck-at fault model is one of widely accepted
model because of having closeness to the actual defects and also, it provide the algorithmic possibilities which, further helps in generation of test vectors. The desired smaller DPM (defective parts per million) levels for devices, creates the need for application of better fault models, which can model the defects in the most accurate fashion. This result in complex fault models which tends to make test generation tedious or even impossible and ultimately increase the test cost. Our motive is to cut down the test cost by finding the minimal number of test vectors for the test. If reduction in the patterns for one module is achieved, it would reduce the overall test cost. We propose universal pattern set which gives good fault coverage for arithmetic circuit with small set of vectors.

References


**Index Terms**

Computer Science

Integrated Circuits

**Keywords**

DFT Universal Pattern Set Test Cost