Abstract

This paper presents the design and implementation of a new Program Address Generator (PAG) unit, which is a part of Program Control Unit (PCU) well suited for DSP Processors. This would be compatible with DSP56002 (DSP Processor from Motorola) at instruction level. The PAG provides hardware dedicated to support loops, which are frequent constructs in DSP algorithm. The proposed architecture of PAG has been modeled, verified and synthesized using VHDL description and synthesis tools. It is found that the proposed AGU generates actual address for program memory as per the given set of inputs. Simulation results are compared with the theoretical data and found correct.

References

Design and Implementation of a New Program Address Generator Unit in a DSP Processor

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