Double-gate FinFET is a novel device structure used in the nanometer regime, whereas the conventional CMOS technology’s performance deteriorates due to increased short channel effects (SCEs). Double-gate (DG) FinFETs has better SCEs performance compared to the conventional CMOS and stimulates technology scaling. In this paper, we are designing 32nm DGFinFETs and extracting their characteristics by using Sentaurus TCAD, Simulated results of the device show that it can be governed at the nanometer-scale regime. DGFinFET has independent gates; threshold voltage of one gate can be altered by varying the voltage at the other gate. By using this phenomenon logic circuit can be configured in one of the modes such as SG mode, LP mode, IG mode and IG/LP mode. INVERTER and NAND gate are designed in the above mentioned node and comparison has been drawn between them. Based on the simulated results SG-mode is adequate for high-performance design.
References

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Index Terms

Computer Science

Integrated Circuits
Keywords
Double-gate Finfet (dgfinfet) High-performance Independent Gate (ig) Mode Logic Gates
Low Power (lp) Mode
Short Channel Effects (sces)
Shorted Gate (sg) Mode