Abstract

This paper presents the PLL based Frequency Synthesizers, which are used in modern devices for generating wide range of frequencies. The Performance depends on several factors such as phase noise, spurious outputs, loop bandwidth and lock time. The parameters loop bandwidth and lock time are inter-related which are inversely proportional to each other is simulated and the results are given. The Phase Noise for the VCO depends on the frequency range in which it is used and given by Lesson’s equation. It varies linearly and L-Band and higher frequencies but varies at 6dB per octave at lower frequencies in hundreds of MHz or tenths of GHz. The results are simulated in MATLAB and presented in this paper.

References

- Ken Holladay, "Design a PLL for a specific Loop Bandwidth", Fujitsu Microelectronics, Oct 2000
- Curtin, Mike and Paul O'Brien, "Phase Locked Loops for high-frequency receivers and transmitters-part 3", Analog Dialogue, 33-7, 1999

**Index Terms**

Computer Science  
Signal Processing

**Keywords**

Frequency Synthesizers  Phase Noise  Lesson's Equation