Abstract

The matrix multiplication is a computationally intensive problem and a prerequisite in various image processing applications like spatial and frequency filtering, edge detection and convolution. Being a core part of various applications in portable devices like mobile phones, demand for high speed and low power consumption is extremely high. This work demonstrates an effective design and efficient implementation of the Matrix Multiplication using Systolic Architecture and Ancient mathematics. For efficient implementation and maximum speed-up, integer arithmetic was used. Three main steps of the work, i.e. design, simulation and implementation, were accomplished. For design and simulation, Verilog HDL was used. The design was simulated using modelsim10.1d and synthesized using Xilinx Planahead 12.1. The work also includes the comparison between three design approaches of the matrix multiplication using systolic architecture. In the first design approach, array multipliers were used. In the second approach, Wallace tree multipliers were used and in the final approach, matrix multiplier design was based on Ancient multiplication technique.

References

- Sumit Vaidya1 and Deepak Dandekar ‘Delay power performance comparison of multipliers in VLSI circuit design’, International Journal of Computer Networks & Communications (IJCNC), Vol. 2, No. 4, July 2010
A Novel Design of Low Power, High Speed SAMM and its FPGA Implementation

- Jagadguru Swami Sri Bharath, Krsna Tirathji, "Vedic Mathematics or Sixteen Simple Sutras From The Vedas", Motilal Banarsidas, Varanasi(India), 1986.

Index Terms

Computer Science  Signal Processing

Keywords

Systolic Architecture  VLSI  Vedic Mathematics