Abstract

The Efficiency of present symmetric encryption algorithms mainly depends on implementation cost and resulting performances. Present symmetric encryption, like the Advanced Encryption Standard (AES) rather focus on finding a good tradeoff between cost, security and performances. Some present symmetric encryption algorithms are targeted for software implementations and shows significant efficiency improvements on these platforms compared to other algorithms. From these algorithms, consider a general context where we have very limited processing resources (e.g. a small processor). It yields design criteria such as: low memory requirements, small code size, limited instruction set, i.e. Scalable Encryption Algorithm (SEA). For this purpose, loop architecture of the block cipher is presented. The total modules of SEA written in VHDL coding, the simulation and synthesis results are verified by the Virtex-4 of Xilinx 9.1i. This paper also carefully describes the implementation details and corresponding area requirements.

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Index Terms

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Keywords

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