Abstract

Digital gates are the basic components of the digital circuits. To reduce the cost of the circuit, number of these gates must be reduced, and hence a method is needed to do the desired. There are some methods such as Karnaugh maps, in which visualization becomes difficult when number of variables become more than five, and Quine Mccluskey method, which overcomes the drawback of Karnaugh maps but it becomes complex when large number of variables are used. Here, in this paper, an approach, Consummate minimizer(C-minimizer) has been proposed which overcomes the limitations of such conventional methods and produces a minimized expression containing minimizing elements. The same can be used in minimizing the patterns in large data sets.

References

- K. J. Dean, "An Extension of the use of Karnaugh Maps in the minimization of logical functions", IEEE in Radio and Electronic Engineer , vol. 35, pp 294-296, may
C – Minimizer Algorithm: A New Technique for Data Minimization


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